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Design of all optical logic half adder based on holes-in-slab photonic crystal

Kamanashis Goswami[1,3] · Haraprasad Mondal[2] · Mrinal Sen[1]

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Abstract
In this paper an all-optical half adder has been designed on a 2D photonic crystal slab having air holes in a hexagonal lattice pattern. The working principal of the device is based on beam interference. Multi-mode interference based Pi phase shifter been used in this design. Neither any nonlinear materials nor any extra bias signal has been incorporated in the structure. Plain wave expansion and Finite Difference Time Domain methods have been used for analyzing the band diagram of the structure and performance of the proposed device respectively. The SUM port provides 60%, 67%, and 1% transmittance whereas the CARRY port provides 4%, 1%, and 90% transmission for {0,1}, {1,0}, and {1,1} logic combinations respectively. Minimum contrast ratio has been obtained as 18 dB in SUM port and 12.5 dB in CARRY port. Therefore, it is expected that the proposed all-optical adder would be a potential candidate for future generation photonic integrated circuits.

Keywords Optical adder · Photonic crystal · Beam interference · Phase shifter · Band diagram

1 Introduction

The demand of high-speed data computation is ever increasing and the conventional electronic processing units are no more capable to fulfil the demand. Therefore, now, it seems to be inevitable to move towards all optical devices/circuits for optimizing the performances of the processing units (Yablonovitch 1987; Baqir et al. 2018; Alipore et al. 2018).

✉ Mrinal Sen
mrinal.sen.ahm@gmail.com

Kamanashis Goswami
kamanashis.goswami@gmail.com

Haraprasad Mondal
mandal.haraprasad@gmail.com

[1] Electronics Engineering, Indian Institute of Technology (ISM) Dhanbad, Dhanbad, Jharkhand, India

[2] Dibrugarh University Institute of Engineering and Technology, Dibrugarh University, Dibrugarh, Assam 786001, India

[3] Haldia Institute of Technology, Haldia, Purba Medinipur, West Bengal 721657, India

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Furthermore, this changeover can also improve the communication system by providing high bandwidth and ultrafast switching speed by avoiding the conversion in between optical to electrical signal. Therefore, to make all the data processing/computation in optical domain, optical devices like logic gates, decoder/encoder, multiplexer/demultiplexer, adder/subtractor, are highly required. To optimize the advantages of optical network/processing unit, the fabricating platforms play crucial role. In this contrast, photonic crystals (PCs) (Farmani et al. 2019, 2020; Goswami et al. 2022a, 2022b, 2023) have drawn the attention of the researchers for its unique characteristic called photonic band gap (PBG) along with its other advantageous features like ultra-compactness, high contrast ratio and low power consumption. PBG is the prohibited range of frequencies of optical signals that cannot propagate through the PCs. However, if a defect is made, by removing a row of rods or holes, a narrow band of permissible frequencies can propagate through the defect which acts as a waveguide. An optical signal/light can be highly confined, in nanometre range, along PC waveguide due to its PBG. In recent past, several logic Gates (Goswami et al. 2022; Fu et al. 2013; Parandin 2017; Mondal et al. 2022, 2015; Failed 2016; Alipour-Banaei et al. 2014, 2017; Fariborz Parandin 2018), and other optical devices (Parandin and Reza 2020; Goudarzi et al. 2016; Goswami et al. 2020a; Pashamehr et al. 2016; Lin et al. 2013) like adder/subtractor (Xie et al. 2017; Goswami et al. 2020b; Abdollahi and Parandin 2019; Neisy et al. 2018; Maleki et al.2020, 2021a, 2021b), encoder/decoder (Mondal et al. 2019a; Salimzadeh and Alipour-Banaei 2018; Kim April 2000; Chen et al. 2006; Chung et al. 2006; Sharma et al. 2022; Moniema 2015; Maleki et al. 2023; Maleki and Soroosh 2020; Makvandi et al. 2022), multiplexer/demultiplexer (Mondal et al. 2018, 2019b; Gogoi et al. 2016; Zhu and Li 2006; Jiu-Sheng et al. 2015; Rostami et al. 2010; Maleki and Soroosh 2022a, 2022b), polarizer (Prakash et al. 2018; Tao Liu et al. 2005) have been designed by moulding, regulating, splitting and converging PC waveguides and optical signals as well, both in linear and non-linear domain. High performing logic devices increases the overall performance of the photonic integrated circuit (PIC). In this context, among various optical logic devices/ switches, a full adder (FA) is a very crucial device. Arithmetic operation like addition, subtraction, multiplication, division etc. can be done using a full adder. A full adder can be designed using two half adders.

In the previously reported nonlinear designs (Neisy et al. 2018; Liu et al. 2008; Alipour-Banaei and Seif-Dargahi 2017; Cheraghi et al. 2018), Kerr effect has been exploited, where the refractive index of a nonlinear material changes with the intensity of light. Hence the operating power is more compared to linear designs. Furthermore, the response time of a device that functions based on a nonlinear optical property is usually large. Moreover, it is also difficult to embed a nonlinear material in a linear material. Inspite of these limitations, contrast ratio of the designs is remarkable. In (Jalali-Azizpoor et al. 2018; Xavier et al. 2013; Jiang et al. 2015), they have made use of self-collimation method for designing a half adder, where the required foot print area is less compared to the aforesaid designs. But, in self-collimation method the power gets divided and hence reduced. Therefore, it incurs intrinsic problem for cascading. In recent past few all-optical HA designs (Abdollahi and Parandin 2019; Karkhanehchi et al. 2017; Parandin et al. 2017; Mahmood et al. 2019; Swarnakar et al. 2016; Serajmohammadi et al. 2018; Pathak et al. 2020) have also been reported, where optical beam interference method has been exploited. The required footprint area and device response time are, in general, less. But the contrast ratio of the designs, as reported, are not attractive. However, various parameters of the aforesaid designs are tabulated in the sub-Sect. 3.4. Moreover, all the reported devices are based on rods in air PhC structure and the slab height has been considered as infinite. Though it is easy to regulate optical signal in rods in air structure, but its mechanical stability is

questionable and it needs a base to hold the structure. The refractive index of the base materials has to be considered and the fabrication process is also hazardous. Infinite third dimension is also an impractical concept. Moreover, here authors would like to mention that, to the best of the authors' knowledge till date no one have proposed the design architecture of optical adder in PhC based holes-in-air platform. To overcome these limitations the authors decided to design a half adder circuit in linear domain based on holes in slab structure, where the height of the slab has been considered as finite. But due to lack of extensive computational facility effective refractive index model (Jamois et al. 2003) has been adopted.

In this paper, a half adder circuit, based on light beam interference, has been designed in holes in slab PhC structure. An MMI based π-phase shifter has been realized by creating a defect in a waveguide by removing six holes from both side of the waveguide. However, in this device we have used holes-in slab PhC structure. The holes-in-slab structure is usually preferred over the rods-in-air PhC structure. In rods-in-air structure dielectric rods are suspended in air. So, it needs a base to hold the structure. Therefore, the refractive index of the base material has to be taken into consideration. Fabrication of such structure with a base is quite challenging. The mechanical stability of rods-in-air structure is also questionable. Moreover, in most of the reported articles the third dimension i.e., height of the structures has been considered as infinite which is not practical for real device. Therefore, it has been decided to design the proposed device in holes-in-slab platform with a finite height. In addition to this, no non-linear materials have been used in this design. It mainly depends on homogeneous materials; thus, their fabrication is more feasible than their nonlinear counterpart. No threshold power is required to initiate the operation of the device. Additionally, the speed-of-response and the footprints of the linear optical devices are lower than that of the nonlinear devices. Moreover, no extra bias signal is required in this design which avoids the design complexity.

The remaining portion of the chapter has been arranged by following this sequence. In Sect. 2, the design of the proposed half adder has been presented. Followed by architectural design of the proposed device, the result and performance metrices have been discussed in the Sect. 3. Finally, Sect. 4 concludes the work.

2 Device design and its operation

The basic structure of the all-optical half adder circuit is shown in Fig. 1. It is designed on a 2D PhC where air holes are arranged in hexagonal pattern in a dielectric material. Here the refractive index of the dielectric materials is taken as 3.46 (Si). The lattice constant (a) and the radius (r) of the holes are considered as 450 nm and 144 nm (0.32a) respectively. The total design involves 41×61 holes that makes a footprint of 486 μm^2.

The application of the PWE algorithm has facilitated the calculation of the band diagram for the Photonic Crystal (PhC), and the results are illustrated in Fig. 2. In Fig. 2a, it can be observed that the band diagram for the non-defective crystal, which reveals the presence of a complete Photonic Band Gap (PBG) ranging from 1325 to 1765 nm in wavelength. This PBG encompasses the standard optical communication wavelength of 1550 nm within its mid-range. Furthermore, we have conducted the calculations to determine the projected band for a W1 line defect along the Γ-M direction of the crystal, which is displayed in Fig. 2b. In this case, the guided band is observed within the wavelength range of 1430 nm to 1630 nm.

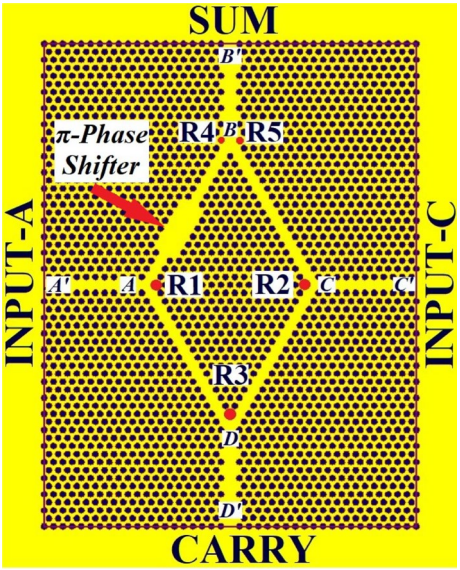

Fig. 1 Structural layout of Half-Adder

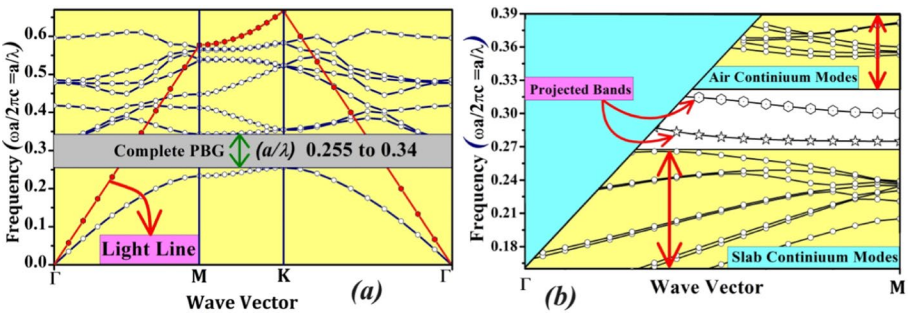

Fig. 2 **a** Photonic band diagram of non-defect structure **b** projected band diagram of defect structure

Moreover, to execute the FDTD simulation process the parameters like time step, grid spacing, and boundary conditions have been taken as 0.014 micro-seconds, Dx = 28 nm Dz = 24 nm and boundary condition = PML (perfectly matched layer) respectively. The structure consists of four waveguide AB, BC, CD, DA, arranged like a rhombus as shown in Fig. 1. All the four waveguides are having same length of 16a which is equal to 7.2 μm. AA′, BB′, CC′, DD′ are four waveguides originated form A, B, C and D respectively. AA′, CC′, AB, BC, CD, DA are all made by removing one row of holes (W1 defect) in ΓM direction. BB′ and DD′ waveguides are made by removing three adjacent rows of holes in ΓK direction. The device consists of four ports namely A′, C′, B′ and D′. Port A′ and C′ are used as input ports of the half adder. Port B′ is used as SUM port and port D′ is used as CARRY port of the device. B′ port (SUM) is HIGH when either of the inputs are HIGH, but LOW when both the inputs are HIGH/LOW. Port D′ is high only when both the inputs are HIGH, and LOW otherwise.

The device is working based on constructive/destructive interference of optical beam (Fu et al. 2013; Fasihi 2016). When two optical signals of same amplitude intersect at any

point in phase, the resultant signal increases, but when two optical signals of same amplitude intersect each other out of phase, they destruct each other. At Junction A and at junction C two holes named as R1 and R2 have been optimized by increasing their radius from r to 1.6r. Input signal, coming from port A′, gets split in junction A and starts flowing towards B and D through the waveguide AB and AD respectively. Almost half (50%) of the input signal coming from A′ flows through AB and another half (50%) of the signal flow through AD. Likewise, optical signal coming from input port C′ gets divided into almost two equal parts at junction C and flows towards B and D through CB and CD respectively. At junction D, one hole named as R3 has been optimized as 1.7r. At junction B two holes namely R4 and R5 have been optimized (red dot) as 0.8r. The junction D has been modified by changing the radius of only one hole such that the junction blocks only one optical signal coming either from junction A or from junction C at a time. But it fails to block the signals if the signals come simultaneously. In terns the junction D works as a AND gate where A and C are its inputs and D′ is the output. In the waveguide AB, one '7a' long W3 cavity has been made, which is basically a multimode interference (MMI) device, as shown in the Fig. 1. This MMI device works as a π-phase shifter. The working principle of the MMI device has been analysed in Goswami et al. 2023. Whenever a signal passes through the cavity (in this case A to B) it gets a π-phase shift. The length of AB and CB are made equal and the length of AA′ and CC′ are also made equal. Therefore, when two optical signals of same phase start flowing from junction A and from junction C towards B, they meet out of phase at B, hence make a destructive interference. Junction B has been optimized so that when an optical signal comes from either of the input ports, the junction should allow the signal to pass smoothly towards the output port B′. In turn the junction B is working as a XOR gate, where A and C are the input ports and B′ is the output port.

Nevertheless, we should discuss the challenges of fabricating the device. CMOS fablabs have matured and advanced to scale down electronic transistors, aiding in silicon-based photonic component fabrication. Literature suggests CMOS processes like E-Beam Lithography (EBL) and Reactive Ion Etching (RIE) are sufficient for holes-in-slab type PhC fabrication. Achieving the required aspect ratio with vertical walls is however challenging. Deep RIE with a hard mask can be fruitful in this regard, but it may increase the wall-roughness, which might not matter significantly for a small-sized component. Nevertheless, the RIE and EBL recipes are required to be optimized for the desired PhC structure. Further, the statistical modeling will mitigate fabrication imperfections including the proximity-effect. We hope these strategies will lead to successful device realization. The process can be summarized as follows.

- Deposition of photoresist for patterning on the target silicon wafer.
- Definition of the design (PhC structures) using e-beam lithography followed by development.
- Etching of the structures using RIE/DRIE.
- Resist ashing/lift-off and cleaning.

3 Simulation result and performance analysis

The simulations have been performed in two platforms, i.e., the commercial software by R-Soft and the other is MIT Photonic Bands (MPB). To observe the electric field profile and to evaluate the performance metrices the FDTD (Huang et al. 1991) algorithm has

been applied. The performance of the device as a half adder can be evaluated by four following cases.

Case 1 When both the input ports (A and C) are not excited with any continuous optical signal, there is no output signal available at any output ports. This can be considered as '00' input state of the half adder.

Case 2 In this case only the input port A′ is exited with a monochromatic continuous optical signal having a wavelength of 1550 nm. The signal, at the junction A, gets divided into two equal parts. One-part (almost 50%) stars flowing through the waveguide AD and appears at point D. But at junction D, R3 hole blocks maximum portion of the signal and only 1% of the signal power appears at the D′ (CARRY) port which is considered to be logic-0 (LOW). Another part of the signal moves towards junction B through AB and appears at port B′ (SUM) with 67% of the input signal power, which is considered as logic-1 (HIGH). Hence the output at port B′ becomes HIGH. The electric field distribution and time evolving graph for this state are shown in Fig. 3a, b respectively. This condition can be considered as 01 input condition of the half adder.

Case 3 For '10' input condition, only input port C′ is excited with a monochromatic continuous optical signal in this case. The optical signal, applied at port C′ gets divided into two equal parts at junction C. Finally, 60% of the optical signal appears at the output port B′ (SUM) through CB and BB′ waveguides which is considered as logic-1 (HIGH). Another part of the signal travels through CD waveguide and major portion of the signal is blocked at junction D. Only 4% of the signal reaches at the output port D′ (CARRY), which is considered as logic-0 (LOW). The electric field distribution and time evolving graph for this input condition are shown in Fig. 4a, b respectively.

Case4 In this case, both the input ports are excited with input signals having same amplitude and same phase. Signal from C′, after being split at junction C, reaches at junction B. At the same time signal from A′ also reaches the junction B. But signal from port A′ makes a 180-degree phase shift while passing through the W3 cavity in waveguide AB. Therefore, both the signal meet at junction B out of phase and a destructive interference occurs between them. As a result, only 1% of the signal power appears at port B′ which makes the SUM logic-0 (LOW). On the other hand, one part (almost 50%) of the signal form A′ and from C′ appear at junction D through AD and CD respectively. Thereafter the combined signal from junction D moves toward port D′. Hence the port D′ (CARRY) delivers 90% of input signal power which is considered as logic-1 (HIGH). The electric field distribution and time evolving graph for this state are shown in Fig. 5a, b respectively. This condition can be considered as '11' input condition.

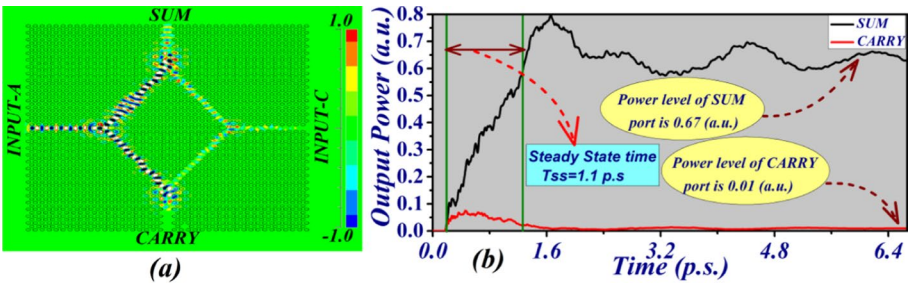

Fig. 3 **a** Field distribution **b** time evolving graph, for logic condition '01'

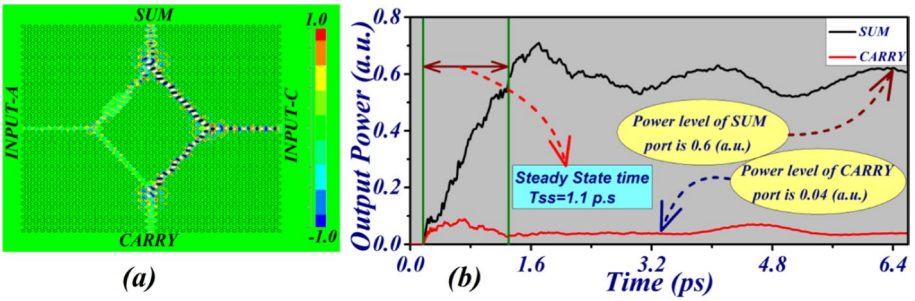

Fig. 4 **a** Field distribution **b** time evolving graph, for logic condition '10'

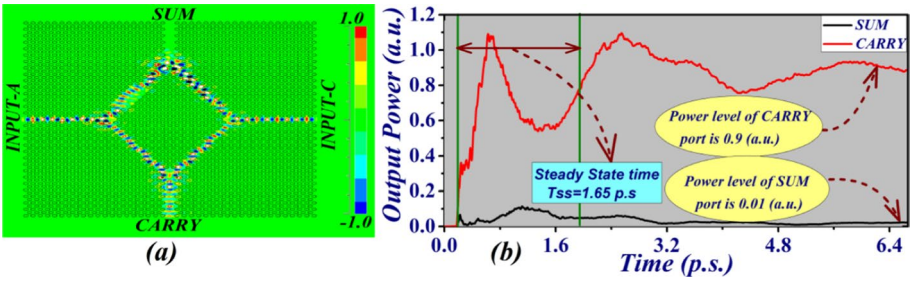

Fig. 5 **a** Field distribution **b** time evolving graph, for logic condition '11'

Table 1 Output logic levels and power levels of half adder for different input logic conditions

Input logic levels		Output logic levels		Normalized output power	
Input-A	Input-C	SUM	CARRY	SUM	CARRY
0	0	0 (LOW)	0 (LOW)	0 Pi	0 Pi
0	1	1 (HIGH)	0 (LOW)	0.6 Pi	0.04 Pi
1	0	1 (HIGH)	0 (LOW)	0.67 Pi	0.01 Pi
1	1	0 (LOW)	1 (HIGH)	0.01 Pi	0.9 Pi

Pi = Input power

Moreover, the logic levels and power levels of all the output ports (SUM & CARRY) have been shown in Table 1. The various performance metrices of the proposed half adder like contrast ratio, bit rate and transmittance have been calculated which are depicted in the following subsections.

3.1 Contrast ratio (extinction ratio)

The definition of contrast ratio (CR), also known as extinction ratio (ER), is the ratio between the power levels of logic-1 and logic-0 at the output ports of the device. The mathematical expression of the contrast ratio is (Singh and Rawal 2015; Shaik and Rangaswami 2016)

$$\text{Contrast Ratio (CR)} = 10\log_{10}(\text{P1}/\text{P0})$$

where, P1 is optical power level at the output port when output power is considered to be logic-1 and P0 is optical power level at the output port for logic-0 condition. One of the important parameters for measuring the performance of the device is contrast ratio, because it is directly proportional to the noise margin and inversely proportional to the bit error rate (BER). Increase in contrast ratio of a device reduces the chance of bit error of the device. Contrast ratio of SUM and CARRY port of the proposed half adder has been calculated as 18 dB and 12.5 dB respectively.

3.2 Response time and bit rate

To calculate the propagation delay and bit rate of the device, response time is another important parameter. Response time consists of transition time (Ttr) and steady state time (Tss) (Singh and Rawal 2015). The transition time is defined as a required time for a signal to reach from input of the device to the output of the device with a power level of 1% of its steady state output. On the other hand, the steady state time is defined as the required time for a signal to reach from 1 to 90% of its steady state output. From time evolving graphs for all possible input logic level condition ('01', '10' and '11') as shown in Figs. 3b, 4b and 5b respectively, the response times have been calculated. From Fig. 3b it has been observed that for '10' input logic conditions the transition time and steady state time are 0.15 pico-seconds and 1.1 pico-seconds respectively. Therefore, the response time for input logic condition (10) is calculated as 1.25 pico-seconds. Moreover, Fig. 4b depicts that for '01' input logic conditions the transition time is 0.12 picoseconds and steady state time is 1.1 picoseconds. Hence, for input logic conditions (01) the response time has been calculated as 1.22 pico-seconds. From Fig. 5b it is clear that the transition time and steady state time are 0.15 picoseconds and 1.65 picoseconds when both the input ports are excited with optical signal. So, in this logic condition (11), the overall response time is calculated as 1.8 pico-seconds. However, in best case scenario the proposed device can be operated with a response time of 1.22 pico-seconds.

The data rate of a device is one of the crucial parameters. To calculate data rate of a device, steady state time is important. For a device the rise time of a signal is equal to steady state time (Tss), but in linear optical domain the falling time of a signal is equal to rise time of that signal. Therefore, to complete a half cycle the required time is calculated as 2xTss. Hence, for the narrow pulse the band-width of the channel is calculated as 1/(2Tss). Finally, for all the possible input logic combinations the transition time, steady-state time and bitrate have been calculated and have been tabulated in Table 2. However, in best case scenario the proposed half adder can be operated with a bit rate of ~ 454 Gbps.

3.3 Transmittance

Transmittance of each of the output ports have been evaluated and shown in Figs. 6a–c for the logic combinations {0,1}, {1,0}, and {1,1}, respectively. The figures show that the device can successfully operate within a 2 nm optical bandwidth cantering at 1550 nm.

Table 2 Transition time, steady state time and data rate of the proposed half adder

Input Signal		Transition Time (T_{tr}) (in ps)	Steady State Time (T_{ss}) (in ps)	Response Time ($T_{tr}+T_{ss}$)	Bit Rate (2xTss)
Input-A	Input-C				
0	0	–	–	–	–
0	1	0.12	1.1	1.22	454 Gbps
1	0	0.15	1.1	1.25	454 Gbps
1	1	0.15	1.65	1.80	303 Gbps

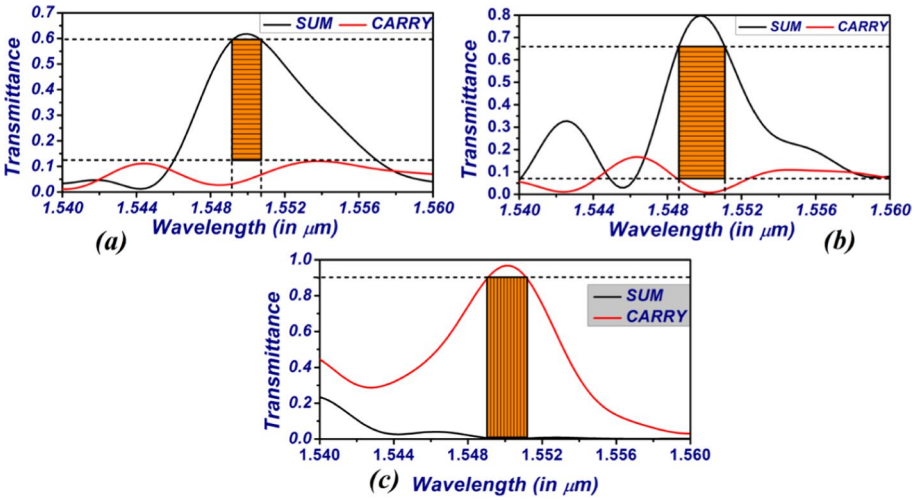

Fig. 6 Transmittance spectra of the SUM and CARRY ports at input logic states **a** {0,1} **b** {1,0} and **c** {1,1}

3.4 Comparative study

The comparative analysis of the works (based on photonic crystal structure) reported earlier has been depicted in Table 3.

4 Conclusion

This work proposes the design of an all-optical half-adder based on holes-in-slab silicon PhC. The light beam interference phenomenon has been used to model the device. The design consists of a rhombus-shaped structure made of four W1 waveguides. One of these W1 waveguides contains the MMI based π-phase-shifter. Two opposite corners of the rhombus are connected with two input ports, while the SUM and CARRY ports are connected to other corners. Two holes at the corner associated with the SUM port are modulated to enhance transmittance, whereas one hole at the corner adjacent to the CARRY port are modified such that the junction can behave as an AND gate. The input beams

Table 3 Comparative analysis of PhC based adders

Refs	Type of the Device	Operating principle	Foot print area	Response time (ps)	Contrast ratio (dB)
Liu et al. 2008)	Half adder	Resonant cavity	70 μm^2	–	Sum-30 Carry-20
Neisy et al. 2018)	Half adder	Resonant cavity	303 μm^2	3	–
Alipour-Banaei and Seif-Dargahi 2017)	Half adder	Ring resonator	439 μm^2	1.5	–
Cheraghi et al. 2018)	Half adder	Resonant cavity	396 μm^2	8	–
Xavier et al. 2013)	Half adder	Self-collimation	169 μm^2	–	Carry-6
Jiang et al. 2015)	Half adder	Self-collimation	278 μm^2	–	–
Karkhanehchi et al. 2017)	Half adder	Beam interference	122 μm^2	–	Sum-5 Carry-3.2
Abdollahi and Parandin 2019)	Half adder	Beam interference	133 μm^2	0.15	Sum-8.4 Carry-9.3
Mahmood et al. 2019)	Half adder	Beam interference	187 μm^2	0.22	Sum-9.3 Carry-8.22
Heydari and Bahrami 2018)	Half adder	BPSK signal coupling	214 μm^2	–	–
Swarnakar et al. 2016)	Half adder	Beam interference	102 μm^2	–	–
Serajmohammadi et al. 2018)	Half adder	Beam interference	1056 μm^2	4	Sum-9.77 Carry-6.98
Pathak et al. 2020)	Half adder	Beam interference	59 μm^2	–	Sum-5.2 Carry-16.7
Maleki et al. 2020)	Full adder	Resonant cavity	115 μm^2	0.40	82% diff
Maleki et al. 2021b)	Full adder	Resonant cavity	71 μm^2	0.39	Sum-13.22 Carry-13.84
This design	Half adder	Beam interference	~420 μm^2	–	Sum-18 Carry-12.5

are split into two halves at the Y-junction ahead of them, formed by two corners of the rhombus. The split beams from both the inputs interfere at the other corners of the rhombus. However, due to the π-phase-shifter at one arm, one set of beams interfere destructively around the SUM port, while the other set interfere constructively around the CARRY port. Thereby, every design component has a role in realizing the adder functionality of the device. FDTD simulations have been performed to establish the operation of the device as a half-adder for all possible input logic states. At the {0,1}, {1,0}, and {1,1} logic combinations the SUM port displays 60%, 67%, and 1% transmittance, respectively; whereas, so for the CARRY port are 4%, 1%, and 90% respectively. The simulation outcomes show a contrast ratio of 18 dB at the SUM port and 12.5 dB at the CARRY port. With such a remarkable performance, the proposed silicon PhC-based all-optical logic half-adder is expected to find in numerous applications in PICs.

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Data availability We don't have any supplementary dataset along with the manuscript.

Declarations

Conflict of interest The authors have no competing interests to declare that are relevant to the content of this article.

Ethical approval We declare that the manuscript entitled "Design of All Optical Logic Half Adder Based on Holes-in-Slab Photonic Crystal" is original, has not been fully or partly published before, and is not currently being considered for publication elsewhere. Moreover, we confirm that no figures and graphs have been reproduced in this manuscript. We further confirm that the order of authors listed in the manuscript has been approved by all of us.

Consent to participate Not applicable.

Consent for publication Not applicable.

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