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Design and analysis of all-optical logic NOR gate based on linear optics

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Abstract
A new design of all-optical logic NOR gate has been proposed in this article based on linear optics. The logic gate has been designed on a two-dimensional holes-in-slab triangular lattice Photonic Crystal structure. Two optical bias signals, each having half unit power have been used to achieve high optical logic state at zero input condition. Finite slab height has been considered to design the proposed device. The Plane Wave Expansion method has been used to calculate the complete photonic band structure of the crystal and projected band of the waveguide. Finite Difference Time Domain method has been applied to measure and evaluate the performance of the device. The simulation results have exhibited high contrast ratio in order of 8.5 dB considering the worst-case scenario. The proposed NOR gate has been implemented as logic inverter and the noise margin of the proposed inverter has also been calculated as 630 μw^2 using Maximum Product Criterion. Finally, the small footprint area of the proposed device, 280 μm^2 and its high operating performance make the device suitable for on-chip photonic integrated circuit applications.

Keywords Photonic crystal · All-optical effect · NOR gate · Light beam interference · Plane wave expansion · Finite difference time domain

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1 Introduction

In the mid of twentieth century, the commercial production of transistors has been started. Since then, an exponential growth of its demand has been observed following the Moore's Law (2015). Every integrated electronic computing and data processing device consists of an enormous density of such transistors and other components with a consequent miniaturization of the footprint and operating power. However, the integration density is eventually heading towards its saturation along with the working efficiency in terms of the operating speed (Keyes 1988). Moreover, presently the world is extremely dependent on digital data exchange and computation. Though, the demand of data exchange rate and speed of computation are increasing at very rapid rate. However, high speed data exchange has been achieved using fiber optic technology, but still problem persists in the data processing nodes due to optical-electronics-optical conversion, which limits the computational speed and increases the signal loss at the interconnects. Therefore, for these above-mentioned drawbacks, the existing technology (Electronics) is incapable to fulfil these enormous demands in near future. In this contest, a cluster of researchers have started embracing a new technology which is 'photonics' (Yablonovitch 1987) and have assured to overcome these limitations of existing technology. Nowadays photonics technology (Yablonovitch 1987) has been adopted in various field of engineering such as communication, manufacturing, biomedical (Deng et al. 2021), aeronautical and so on. Photonics is considered to be the most effective technology with a very high potential as on date and is believed to be used for designing the components of high-speed computation devices (Mondal et al. 2019a, b) in near future for high-speed data processing. Owing to the need of the hour, numbers of cutting-edge developments are going on in different sections of photonics like generation, detection, propagation/processing of optical signal as well as regarding the designing platform (Xue et al. 2019; Li et al. 2018; Xu and Nieto-Vesperinas 2019). In recent past some photonic devices (Baqir et al. 2018; Alipore et al. 2018; Parandin et al. 2018; Mondal et al. 2018a; Farmani et al. 2019; Datta 2018), have been reported where optical waveguides are the key component of those designs. In those designs, some basic optical principles like self-phase modulation (Tomlinson et al. 1984), cross-phase modulation (Olsson et al. 2000), light beam interference (Fu et al. 2013), stimulated Raman scattering (Sen and Das 2013), plasmonic effect (Farmani et al. 2018a, b; Farmani 2019) etc. have been exploited. Among the existing photonic technology, photonic crystal (PhC) (Joannopoulos et al. 2008) is considered to be the most promising design platform of photonic integrated circuit (PIC) (Datta and Sen 2020; Prakash et al. 2018a; Goswami et al. 2020). PhC is refractive index modulation of dielectric material in either one, two, or three dimensions, and it exhibits a unique property known as photonic bandgap (PBG) (Yuan and Lu 2006). PBG is prohibited range of frequencies where light can't propagate through the crystal. However, light, in PBG range can be propagated if defects are made within the crystal. Defects are made by removing or modifying rods or holes of the crystal. In the last couple of decades, a lot of research works have been reported based on the two-dimensional photonic crystal (2D-PhC) like adder (Karkhanehchi et al. 2017; Cheraghi et al. 2018; Neisy et al. 2018; Serajmohammadi et al. 2018; Goswami et al. 2021), subtractor (Parandin et al. 2017), multiplexer and de-multiplexer (Gogoi et al. 2016; Talebzadeh et al. 2017; Banaei et al. 2013; Mehdizadeh and Soroosh 2016a), comparator (Serajmohammadi et al. 2019), polarizer (Prakash et al. 2018b), beam splitter (Noori et al. 2017), filter (Qiang et al. 2007), decoder (Mehdizadeh et al. 2018, 2016, 2017; Daghooghi et al. 2018; Sharma et al. 2022), logic gates (Mondal et al. 2015, 2016, 2018b; Parandin and Moayed 2020;

Parandin and Reza 2020; Goswami et al. 2022) etc. Among all the reported optical devices/logic gates, the Universal NOR gate is considered to be effective one as it can be used as any other basic logic gates and serves as a multipurpose device. Memarzadeh Isfahani et al. (2009) have proposed an all-optical NOR gate based on two non-linear micro ring resonators. In their design two-dimensional photonic crystal with dielectric rods suspended in air type geometry has been used. The two-dimensional finite difference time domain (2D-FDTD) method has been used to measure the performance of the device since the out-of-plane dimension is considered to be extended to infinity which is precisely the height of the rods. However, out-of-plane dimension should be finite so far as the practicality of the designs is concerned. In this context, it is worth mentioning here that the consideration of the finite thickness of the photonic crystal, as in the case of a PhC slab, decides the characteristics which in otherwise is quite different. Isfahani et al. have demonstrated an operating pump power as high as 15.5 w/μm which is evidently not suitable for PICs and it offers low data rate as 333 Gbps. Similarly, another non-linear design of NOR gate has been proposed by Hamed Alipour-Banaei et al. (2014). This design is also based on 2D-PhC of rods-in-air structure with infinite rod height. Since the function of the device is based on nonlinear Kerr effect, it requires high pump power of 2 Kw/μm^2. The operating speed of the device is also lower substantially. Another similar design of AONOR gate in non-linear PhC domain has been proposed by Andalib et.al in (2009). They have used silicon nanocrystal as nonlinear material with Kerr coefficient 10-16m^2 W^{-1}. In their design five nonlinear ring resonators one common waveguide (one end is considered as probe input and other end is considered as output) and two input waveguides have been designed. They have used 1550.8 nm wavelength as input signal and 1568 nm as probe signal. As per the authors, probe signal is always ON and when any one of the input signals is ON then ~ 6% (logic-0) of probe signal appears at the output port whereas ~ 3% (logic-0) probe signal appears at the output port when both the input signals are ON. When both the input signals are OFF the 79% of probe signal appears at the output port which comprises as logic-1. The contrast ratio and bit rate of their device have been reports as 11.19 dB and 138.9 Gbps respectively. Wen-Piao Lin et.al (2013) have proposed a structure of AONOR gate which is similar to the design proposed by Babak Memarzadeh Isfahani et.al. (2009). This device is designed on 15 × 15 square lattice with lattice constant of 630 nm. The radius and refractive index of dielectric rods are chosen as 133 nm and 3.39 respectively. On the other hand, Jibo Bai et al. (2009) and Junjie Bao (2014) have proposed optical NOR gate based on the principle of linear optics. 2D-PhC with rods in air structure has been used to design their devices. The length of the device has been reported in Bai et al. (2009) as 37 μm which limits the response time and data rate of the device. The contrast ratio between two logic levels for both the devices has been reported to be approximately 4.5 dB in best case scenario. Furthermore, Farhad Mehdizadeh et al. (2016b) have proposed a 3-input optical NOR gate based on 2D-PhC rods-in-air platform. Their design is pretty attractive but main drawbacks of this design are its nonlinearity and infinite height of rods. However, it is important to note that most of the designs of optical NOR gate reported in recent past are based on PhC rods in air structure which incur mechanical instability. Furthermore, reported NOR gate designed in nonlinear optics which offers drawbacks like high operating power, requirement of threshold power, long interaction length with the matter, etc. which altogether restrict the device efficiency. This, in turn, motivates the author to investigate the design of an all optical NOR gate exploiting the principles of linear optics in PhC platform of air holes in dielectric slab type geometry, which is expected to offer fast response time, lower operating power and higher contrast ratio between the output logic levels. The simulation results establish that the device offers high contrast ration and can be

operated with a high data rate in the order of 8.5 dB and 500 Gbps respectively. The band diagram of the device depicts that the proposed device is suitable for operation in 1550 nm wavelength which is standard 3^{rd} optical window as per ITU.

The remaining portion of the paper is arranged as follows. The detail design of the proposed device has been described in Section two including the necessary characterization. In the next section, the performance of the proposed NOR gate has been analysed and parameters like response time, data rate, extinction ratio and noise margin of the proposed device are calculated. Finally, the paper concludes in section four.

2 Device design and operating principle

Architecture of the proposed all-optical NOR gate, as has been shown in Fig. 1, is designed based on a 2D-PhC slab. The PhC is configured using air holes that are perforating a silicon slab in a hexagonal arrangement. The lattice constant (a) of the PhC is chosen as 480 nm and the radius of the air holes is considered as 0.32a. The device is designed with a 26 × 47 array of air holes on silicon slab, which altogether provides footprint area of 280 μm^2. The proposed device comprises of two input ports (A and B), two bias ports (Bias-1 and Bias-2) and one output port. Both the bias ports are excited with continuous wave optical signals irrespective of the input logic combinations. Five waveguides (W1 to W5) have been created by means of line defects in the Γ-X direction of the PhC. The waveguides W1 and W2 are placed in parallel at a distance 0.86616a. The input waveguides W1 and W2 intersect with the bias waveguides W3 and W4 at junctions C1 and C2 respectively at an angle of 60 degree. Here, lengths of the waveguides are calculated so that an optical input signal interacts destructively with the bias signal at the junctions C1 and C2. Furthermore, both the bias waveguides W3 and W4

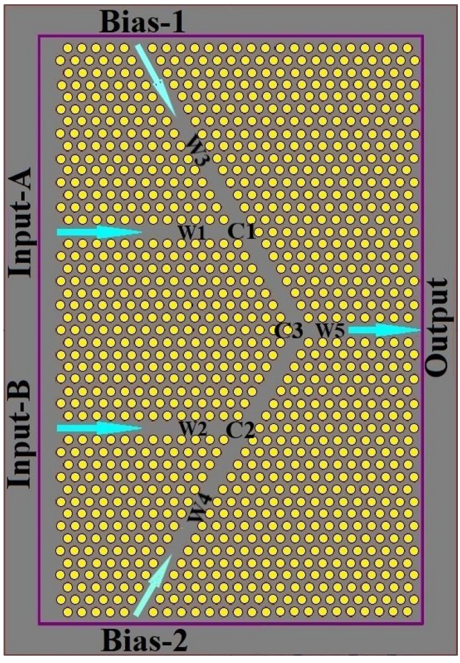

Fig. 1 Schematic diagram of Universal NOR Gate

meet with the output waveguide W5 at junction C3. The length of C1C3 and C2C3 are chosen as 8a. The signals coming from junction C1 and junction C2 make a constructive interference at junction C3 and transmitted to the output port. To calculate the photonic bandgap (PBG) of the bulk PhC and the dispersion diagram of the PhC waveguides (W1-W5), the effective refractive index approach (Huang et al. 1991) has been adopted. The effective index of the slab has been calculated as 2.79. Thereafter, 2D PWE method (Jamois et al. 2003) has been used to calculate the PBG which is shown in Fig. 2a. A bandgap in transverse electric (TE) mode has been obtained with normalized frequency (f= a/λ) ranging from 0.255 to 0.33 (1455 nm to 1880 nm). The dispersion diagram of the waveguides has been shown in Fig. 2b. It can be observed from the Fig. 2b that two bands within the PBG of TE mode are allowed to propagate through the waveguide. The input ports (A and B) are excited with unity power (Pi) signal whereas the bias ports are excited with half unity power (0.5Pi) signal. Afterward, simulations have been carried out using the two-dimensional full vector FDTD method (Johnson and Joannopoulos 2001) in order to study the response of the proposed device for various input logic combinations. The field distribution for different input logic combinations is shown in Fig. 3a–D. The Fig. 3a shows that the proposed NOR gate delivers 0.99Pi power (considered as logic '1') at the output port when neither of the input signals are applied at the input ports (Except the bias signals are which are always present throughout the operations). On the other hand, the output is low when either or both of the inputs are at logic high, which can be seen in Fig. 3b–d. In the cases when output is low, merely 0.02Pi to 0.14Pi of input power are transmitted to output port. The output signal power for various input logic combinations are tabulated in Table 1.

3 Results and performance analysis

The distribution of the electric fields for different logic combinations are used to analyse and calculate several parameters like power variation, response time/data rate, and extinction ratio (ER) of the device. These have been discussed in the following subsections.

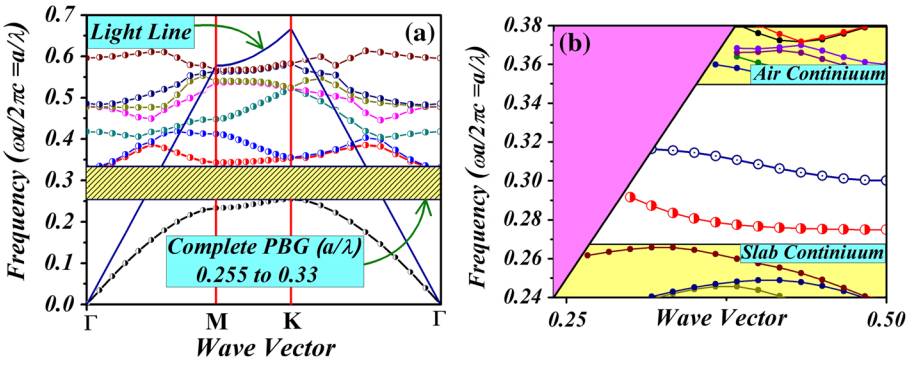

Fig. 2 Dispersion diagram of the photonic crystal structure for **a** TM mode without defect, **b** TM mode in line defect

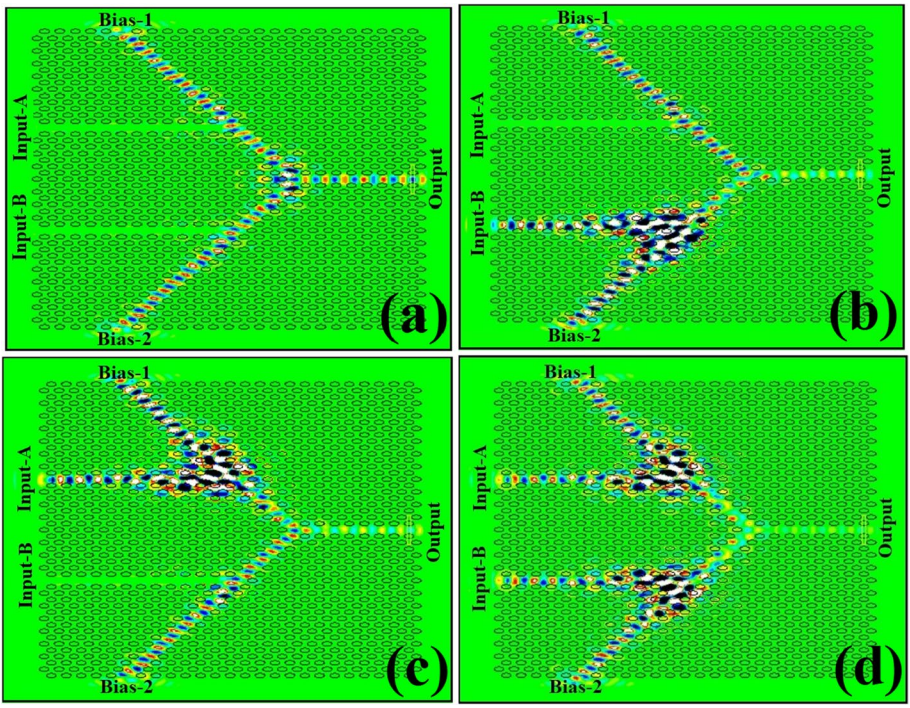

Fig. 3 FDTD Simulation performances of electric field of 1550 nm wavelength where **a** no signals are applied at input ports depicting logic-00, **b** signal is applied at input port B depicting logic-01 **c** signal is applied at input port A depicting logic-10 **d** signals are applied at both the input ports A and B depicting logic -11

Table 1 Truth Table and output power level of NOR gate

Input signal (1550 nm)		Logic level at the output	Power level at the output
Input-A	Input-B		
0	0	1	$0.99P_i$
0	1	0	$0.14P_i$
1	0	0	$0.14P_i$
1	1	0	$0.04P_i$

3.1 Power variation

To analyse the power variation, the behaviour of output power with the variation of input power has been calculated which has been depicted in Fig. 4. When both the input ports (A and B) are set to zero, and only bias signals are present, a signal having power of 99Pi is delivered to the output port. Initially, both the bias ports are fed with constant signal power (0.5Pi). Thereafter, the power of the input signals at both the ports A and B are varied equally and simultaneously from their null values to their final values. Figure 4a shows that when the power of the input signals at both the ports are zero, the output port receives 99% of the input signal power (0.99Pi). Now, as the input signal power increases, the output

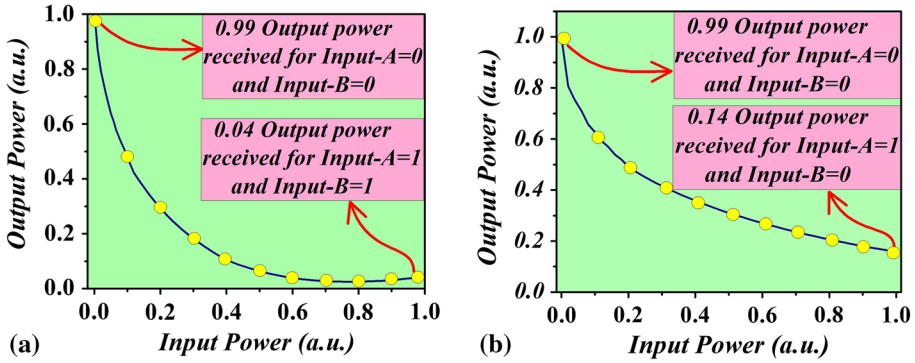

Fig. 4 Graphical representation of power variation in TE mode where **a** power of both the inputs ports A and B are simultaneously varied **b** power of only single input port is varied

power goes on decreasing owing to the destructive interference at the junctions C1/C2. Thus, the output power (P0) decreases with the increase in the input signal power (Pi). However, a very small portion of input signal power (4%) manages to reach to the output port without any obstruction, as shown in Fig. 4a. Thereafter, the input power at port B is set to zero and the input signal power of port A is varied from its null value to its maximum value. Figure 4b shows the variation of output power (P0) with the variation of input power (Pi) at port A. As input signal from port A meets the bias signal (bias-1) at junction C1 in a destructive interference, output power decreases as input power (Pi) at port A increases. However, Fig. 4b depicts that when input signal at port A is set to its maximum value then maximum destructive interference can be seen between bias-1 signal and signal of input port A at the junction C1. However, merely 0.14Pi power appears at the output port under this condition. The device offers similar result when input A is set to zero and the input signal power of port B is varied from its null value to its maximum value.

3.2 Response time and data rate

The response time of a device is another crucial parameter which determines the propagation delay and data rate of the device. Response time has two parts namely transition time 'Ttr' and Steady-state time 'Tss' (Rani et al. 2016). The time taken for a signal to reach at the output from the input after initiation is defined as Transient time 'Ttr', whereas steady-state time 'Tss' is defined as the time taken by a signal to attain at least 90% of its stability after elapsing the transition time. Here, the calculations of the response time have been done from their transient responses, where the average optical power at the output port has been evaluated from the curve of the output power evolving with time. Four different simulations have been performed for the analysis of transition time'Ttr' and steady-state time 'Tss' for a set of various input signal combinations, which are shown in Fig. 5. Different values of transition time and steady-state time for different input combinations are depicted in Table 2. Figure 5a shows that, when there is no input signals, only bias signals are present, transition time (Ttr) and the steady- state time (Tss) are measured as 0.15 ps and 0.12 ps respectively. From Fig. 5b and c it is seen that when either of the inputs (A or B) is ON, Ttr and Tss are observed as 0.15 ps and 0.88 ps respectively. Nevertheless, when both the inputs are ON then Ttr is measured as 0.15 ps and Tss is measured as 0.92 ps as

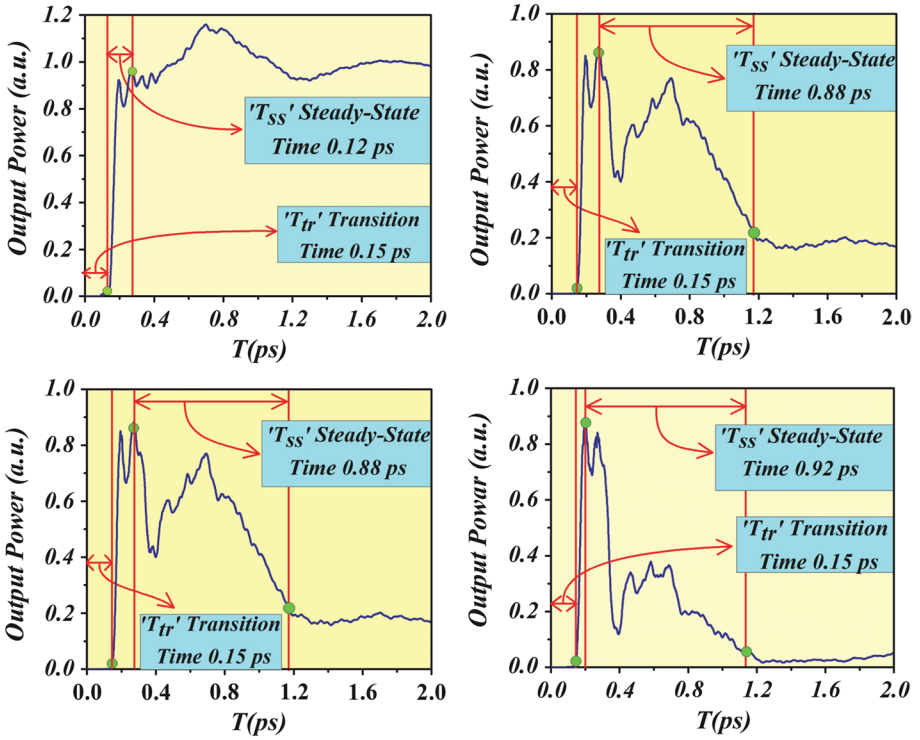

Fig. 5 The output power time-evolution graph when TE signal/s is/are **a** absent to both the input ports, **b** applied to input port-B only, **c** applied to the input port-A only **d** applied to both the input ports

Table 2 Transient time, steady state time, band-width and bitrate of the proposed NOR gate

Input Signal		Transition Time (ps)	Steady State Time (ps)	Bandwidth (THz)	Bit Rate (Tb/s) RZ 1 Hz = 0.5 (bits/s)	Bit Rate (Tb/s) NRZ 1 Hz = 1 (bits/s)
A	B					
0	0	0.15	0.12	4.17	2.08	4.17
0	1	0.15	0.88	0.568	0.284	0.568
1	0	0.15	0.88	0.568	0.284	0.568
1	1	0.15	0.92	0.544	0.272	0.544

shown in Fig. 5d. Thus, in the worst-case scenario, the large response time of the device is found to be 1.07 ps. On the other hand, the steady-state time'Tss' is very important parameter to calculate bandwidth and bit rate of the device. From Fig. 5a it can be seen that the steady-state time is 12 pico-seconds corresponding to logic'0' for both the inputs. Moreover, the falling time of the signal is also expected to be same as rise time i.e., 12 pico-seconds owing to the linear optical regime of operation However, for the linear optical regime operation of the device, the falling time of the signal is also expected to be same as rise time, i.e., 12 ps. Hence, for the narrow pulse the band-width of the channel is calculated

as 1/(2Tss) which is equal to 4.17 THz. It is emphasized here that this bandwidth becomes precisely equals to the bit rate for non-return-to-zero (NRZ) systems; while for the return-to-zero (RZ) systems, the bit rate becomes half of that i.e., 2.08 Tbps. Finally, the transition time, steady-state time, band-width and bitrate (both RZ and NRZ system) for all the possible input logic combinations have been calculated from (Figs. 5a–d) and have been summarized in Table 2. However, in worst case scenario the proposed device is considered to have the ability to operate at a bit rate of ≈ 550 Gbps.

3.3 Extinction ratio (ER)

Extinction ratio (ER), also known as contrast ratio (CR), is defined as the ratio between the output power levels corresponding to logic'0' and'1'. Mathematically, the extinction ratio of a device can be expressed as—ER = 10log10(P1/P0) where, P1 and P0 are the optical signal power at the output at logic-1 and logic-0 respectively. The ER is an extremely crucial parameter in order to characterize the performance of any logic device in terms of the noise margin and bit error rate. Noise margin provides noise tolerances for the logic levels when the device is exposed to signal perturbation due to noise, and the noise immunity of the logic device increases with the noise margin. Increase in the extinction ratio of the device improvises the noise margin which simultaneously reduces the bit error rate (BER). The extinction ratio of the proposed NOR gate has been calculated to be ≈8.5 dB in worst case scenario.

3.4 NOR gate as logic inverter

Keeping in mind the universality of the NOR gate in synthesizing other logic functionalities, the proposed NOR gate can be used to realize logic inverter after modifying its architecture suitably, as shown in Fig. 6. In doing so, a 3 dB power splitter needs to be employed at the input end of the proposed device to distribute the power of the input signal equally to both the input ports of NOR gate. When no optical signal (logic'0') is applied at the input port of the 3 dB splitter; the bias signals deliver the substantial optical power to the output port which suffices for logic'1' at the output. On the other hand, when optical signal is applied at the input port of the 3 dB splitter (logic'1'); the signal gets distributed equally to both the input ports A and B. The two signals get interfered destructively

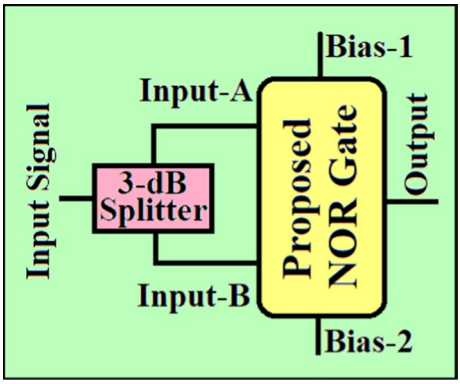

Fig. 6 Block diagram representation of NOR gate as logic inverter

and, consequently, the output is found to be logic'0'. The extinction ratio (ER) of the logic inverter has been.

calculated and it is found to be substantial high in the order of ≈17 dB (where, P1 and P0 are considered as 0.99 and 0.04 respectively). Moreover, to ensure the cascadability of logic inverter in a PIC, the noise margin plays a vital role and has also been calculated. Here, the noise margin has been calculated using maximum product criterion (MPC) (Hauser 1993) which is essentially based on maximizing area of the rectangle inside the loop of the cross-coupled power transfer characteristic (PTC) pair, as shown in Fig. 7 after interchanging the input and output axes. From Fig. 7, it can be seen that two maximum-area rectangles are fitted within two loops which have been formed due to intersecting between curves of PTC and inverse PTC and rectangles are fitted such that two diagonal corners of the rectangle touch the curves. The various parameters of the inverter such as PIL (maximum input power level for logic'0'), PIH (minimum input power level for logic'1'), POL (maximum output power level for logic'0'), POH (minimum output power level for logic'1'), have been measured from graphical representation of the rectangles. Here, the values of PIL, PIH, POL and POH have been found in the order of 15 μW, 720 μW, 7 μW and 795 μW respectively. Additionally, the rectangle in the upper loop represents other few important parameters 220 to calculate the noise margin of the logic inverter. Here, width of the rectangle represents the noise margin low (NML), height of the rectangle represents the noise margin high (NMH) and area of the rectangle represents noise margin product (NMP) (which is considered as noise margin of the logic inverter). The values of NML, NMH and NMP using MPC are found to be 7 μW, 90 μW and 630 μW ^{2} respectively. From figure-7 it can be noticed that NMH is higher enough with compare to NML owing to exponential nature of PTC of logic inverter. However, the proposed logic inverter satisfies the relation POL ≤ PIL ≤ PIH ≤ POH. Hence, it proves that the proposed logic inverter has a potential for cascadability with substantial tolerance in noise for both the logic levels. Now, two maximum-area rectangles are fitted within two loops which have been formed due to intersecting between curves of PTC and inverse PTC and rectangles are fitted such that two diagonal corners of the rectangle touch the curves. The various parameters of the inverter such as PIL (maximum input power level for logic '0'), PIH (minimum input power level for logic '1'), POL (maximum output power level for logic '0'), POH (minimum output power level for logic '1'), have been measured from graphical representation

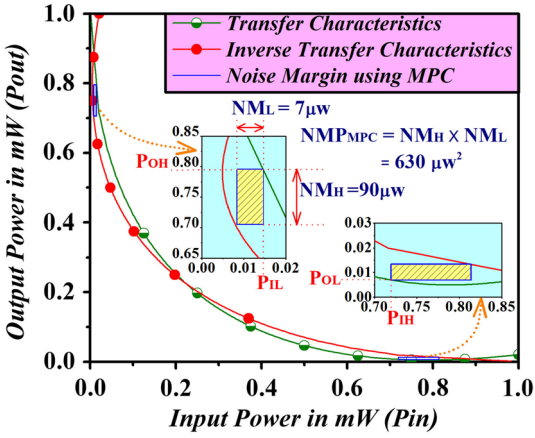

Fig. 7 Noise margin calculation using MPC method

of the rectangles. Here, the values of PIL, PIH, POL and POH have been found in the order of 15 μW, 720 μW, 7 μW and 795 μW respectively. Additionally, the rectangle in the upper loop represents other few important parameters to calculate the noise margin of the logic inverter. Here, width of the rectangle represents the noise margin low (NML), height of the rectangle represents the noise margin high (NMH) and area of the rectangle represents noise margin product (NMP) (which is considered as noise margin of the logic inverter). The values of NML, NMH and NMP using MPC are found to be 7 μW, 90 μW and 630 μW^2 respectively. From figure-7 it can be noticed that NMH is higher enough with compare to NML owing to exponential nature of PTC of logic inverter. However, the proposed logic inverter satisfies the relation $POL \leq PIL \leq PIH \leq POH$ hence it proves that the proposed logic inverter has a potential for cascadability with substantial tolerance in noise for both the logic levels.

3.5 Comparative study

The all-optical NOR gates reported in Isfahani et al. (2009); Alipour-Banaei et al. 2014; Andalib and Granpayeh 2009; Lin et al. 2013; Bai et al. 2009; Bao et al. 2014; Mehdizadeh and Soroosh 2016b) are designed based on 2D-PhC platforms made of a suspended array of silicon rods, arranged in a hexagonal/square lattice in the background of air. The materials used for designing these devices are having different types of refractive indices. Fabrication of such rods-in-air PhC structures with different refractive indices is indeed challenging. Additionally, rods-in-air PhC structure with a finite height incur mechanical instability. On the other hand, in Isfahani et al. (2009); Alipour-Banaei et al. 2014; Andalib and Granpayeh 2009; Lin et al. 2013), some nonlinear materials have been used for realizing ring-resonator/ micro-cavity based NOR gates. As these devices are designed based on nonlinear materials, they suffer from the intrinsic drawbacks of optical nonlinearities, like the requirement of—high operating power, and large length for light-matter interaction. On the contrary, the proposed device is designed based on a 2D-PhC platform that is made of an array of air-holes on a silicon slab. Such a structure, unlike the aforesaid designs, does not suffer from mechanical instability. Moreover, the design architecture of the proposed device is sufficiently simple to fabricate using the matured CMOS fabrication technologies. Finally, and most importantly, the device operates based on linear optics, and hence offers several advantages such as—fast response time, low operating power, small footprint area, and high-power contrast ratio. Nevertheless, as the working principle of the device is based on light beam interference, its operation is severely sensitive to the phase and wavelength of the input signals.

4 Conclusion

This paper presents a new design of an all-optical NOR Gate in a 2D PhC platform based on linear optics. The structure is made of PhC structure of air holes in silicon slab geometry. The device operates at the standard 1550 nm wavelength. The two-dimensional full vector FDTD method has been employed to calculate the performance metrics like power variation; contrast ratio; response time and data-rate. Owing to its linear optical operation and small footprint area, which is in the order of 12.5 μm × 22.5 μm, the device delivers fast response time ≈ 0.99 ps that leads to high data rate of ≈550 Gbps. It also provides a substantial high contrast ratio in the order of 8.5 dB in worst case scenario. Additionally, a

strategy has been shown to operate the proposed NOR gate as a logic inverter. Moreover, the noise margin, which is usually missing in most of similar works; but an important criterion in assuring the success of such a gate in a long chain of similar devices, has also been explored in this work. The MPC criterion is used here to calculate the noise margin of the inverter, which is found to be 630 μw^2. Further, to summarize, the proposed NOR gate has the advantage of being optically linear in operation and is equipped with several potentialities like—small footprint, high-rate data transmission, finite noise margin, cascadable with similar devices, and high contrast-ratio between its logic levels. Owing to these potentialities, the proposed universal gate is expected to be suitable for implementing complex Boolean logic circuits and optical signal processing operations in PICs.

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Declarations

Conflict of interest We wish to confirm that there are no known conflicts of interest associated with this publication.

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