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Impedance matching theory to design an all-optical AND gate

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Abstract: An impedance matching theory-based methodology is presented in this study for designing/optimising photonic crystal-based all-optical AND gate. A basic architecture for the AND gate is projected first, and thereafter the same is optimised utilising the proposed methodology. Performance of the AND gate is evaluated based on several metrics that are calculated using a finite-difference-time-domain simulation. The optimised AND gate has exhibited a high extinction ratio in the order of 6.9 dB, within a very small footprint of $\approx 110\,\mu\text{m}^2$. It also supports propagation of a high bit rate (≈1 Tb/S) and has a wide operational bandwidth (≈4 THz), which make the device suitable for different photonic integrated circuit applications.

1 Introduction

Density of integration and speed of operation of electronic devices are rapidly driving to their saturation, as the miniaturisation of electronics is approaching to the atomic level of silicon [1]. In this context, 'photonics' is one of such technologies which promise to remove these limitations. A long and sustained research in this area has well nourished this technology to make it capable of delivering potential components for photonic integrated circuits (PICs) [2] such as amplifier [3], multiplexer and demultiplexer [4, 5], decoder [6], logic gates [7], polariser [8]. However, it is quite challenging as well as crucial to mould the flow of light in photonics, and majority cluster of researchers depends on photonic crystal (PhC) [2, 9–11] structures for the same. This is because, the geometric arrangement of the lattice of a PhC, which offers a photonic band gap (PBG) for guiding the wave, can easily be modulated to control the optical propagation of a desirable band of frequencies. Thus, recently a number of researchers have reported PhC-based photonic switches and logic components [12–14] for the future generation PICs. Among these, the Boolean logic component AND gate is inevitable for many applications and, hence, different structures have been proposed towards its design. For example, Andalib and Granpayeh [13] have proposed an all-optical AND gate based on Kerr non-linear PhC ring resonators, which supports a data rate of ≈120 Gbps. Similarly, Pashamehr *et al.* have also reported [15] an all-optical AND/OR/NOT gate based on PhC ring resonators utilising the Kerr non-linearity. However, due to non-linearity, these devices require considerable amount of powers for its logic inputs to maintain a sustained extinction ratio (ER), as well as their operations. On the other hand, linear photonics do not demand a minimum threshold of input powers, but designing logic devices in linear optical regime is quite challenging. In this regard, Younis *et al.* have shown [16] operations of all-optical OR and AND gates in linear optical regime using a combination of ring cavity and Y-shape line defect coupler. Fasihi [17] has proposed a simple design of square-lattice dielectric-rod PhC structure, where a dielectric rod has been placed in the junction of the two input-waveguides to implement an all-optical AND gate that has an ER of 6 dB. However, the device cannot perform well in the long chain of similar circuitries as the maximum output power, at a logic '11' input, is merely 50% of its input power. Similarly, Rani *et al.* [18] have designed an AND gate using a 2D air-hole triangular lattice PhC with a point defect in the junction. However, the ER of the gate is <6 dB and also the supporting bit rate of the device is sufficiently low (≈0.8 Tbps), as the wave propagates through a high refractive index material. Although the developments in this field have addressed several important aspects but, still, there is a sufficient space for further improvements. Particularly, to the best of the authors' knowledge, none of these works have devised any generalised methodology for designing/optimising all-optical logic gates, especially AND gates. These motivations have driven the authors to figure out a generalised methodology for designing PhC-based all-optical AND gates, which has been reported in this paper. The methodology uses the impedance matching theory that can be extended for designing other types of all-optical logic gates. To demonstrate the methodology, the work first proposes a design of an all-optical AND gate based on a two-dimensional PhC structure made of a hexagonal arrangement of silicon rods in the air background to make it suitable for fabrication using the standard process technologies. Thereafter, the design is conceptually divided into two parts and impedances of these parts are calculated. A structural parameter is identified and its geometrical property is varied for adjusting impedances. Henceforth, the same is tuned to match (mismatch) the impedances in desirable (undesirable) conditions to make the structure behave like an AND gate. Performances of the gate have been analysed in different wavelength regime, especially in the standard telecommunication band centred at the 1.55 μm wavelength. The same exhibit attainment of a high contrast ratio and remarkable bit rate which are in the order of 6.9 dB and 1 Tb/s, respectively. In a long chain of similar components, the AND gate becomes completely cascadable in terms of frequency and power, which is confirmed from its transmittance (TR) characteristics. Not the least, the ultra-compactness, the absence of power threshold, and the wide bandwidth of the gate make it a potential candidate as a most basic component for the future generation PICs. It is expected that such designs also have the potentiality to play an important role in the future of high-speed optical communication systems [19].

This paper is arranged into three sections: Section 2 details the basic architecture for the AND gate and presents the design principle based on the impedance matching theory. Section 3 evaluates the performances of the AND gate based on its power transfer, propagation profile, ER, TR and response time. Finally, a conclusion on the work is drawn in Section 4.

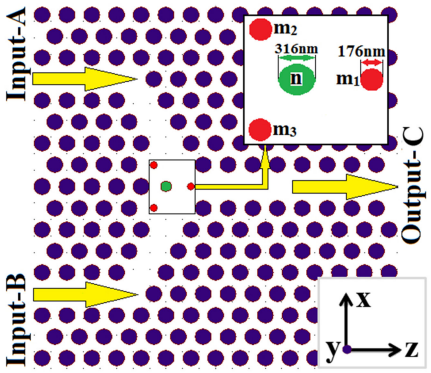

Fig. 1 *Schematic structure of 2D PhC AND gate*

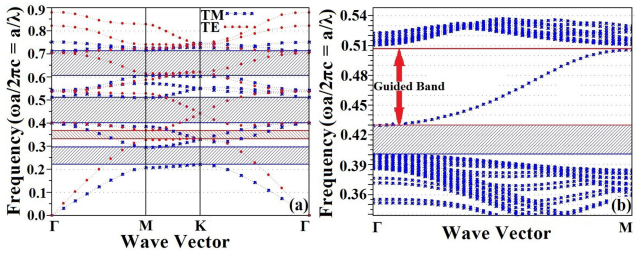

Fig. 2 *Dispersion diagram of the PhC structure for*
(a) TE and TM modes without defect, ***(b)*** line defect projected band in TE mode

2 Basic device architecture and impedance matching theory-based design principle

The basic structure of the proposed AND gate is shown in Fig. 1. It is designed based on a two-dimensional (2D) PhC platform considering a suspended array of silicon rods, arranged in a hexagonal lattice in the background of air. The lattice constant (a) of the PhC is considered to be 740 nm and the radius of the rods is taken as 0.32a. Footprint size of the total device becomes merely 110 μm^2 as it involves 17 × 15 number of PhC cells. A 2D plane wave expansion (PWE) [20] method is applied to obtain the dispersion diagram of the structure. The PWE has analysed the non-defect PhC and explores complete band gaps for both the transverse electric (TE) and transverse magnetic (TM) modes, which are depicted in Fig. 2a. It can be seen from the figure that the band gaps for the TM and TE modes are in the normalised frequency (a/λ)-range 0.40–0.51 and 0.332–0.368, respectively. Moreover, the projected band analysis along a W1 line-defect waveguide within the structure is also performed and is shown in Fig. 2b along with the TM band gap. The figure shows that a W1 waveguide along the 'Z' direction of the structure allows TM mode propagation in a wide range of wavelengths ranging from 1465 to 1720 nm (corresponds to 0.505–0.43 in the a/λ scale). This large range of wavelengths includes the 1550 nm, which is a standard optical communication wavelength as per the international telecommunication union and is chosen as the operating wavelength of this work.

The device, as shown in Fig. 1, consists of two input ports, termed as A and B, and an output port, termed as C. Now, to couple the powers available at the input ports and to transfer this coupled power to the output port, a Y-shaped channel waveguide is designed by implementing W1 line defects. The W1 line defects from/to the ports are formed by removing single rows of rods in the 'Z' direction. Thereafter, the Y junction is formed by removing two rows diagonally from the end of the input waveguides to the junction initiating the output port. The junction actually forms a cavity as described in Fig. 3, however yet un-optimised for the desired performance, as the output receives a significant portion of the input power whenever (any-one or both) the inputs are excited with the operating wavelength.

Now, the cavity needs to be optimised such that the component behaves like a AND gate, i.e. logic 'High' is received at the output port only when both the input ports are fed with logic 'High'. Here, the logic levels are represented by the power levels, and hence

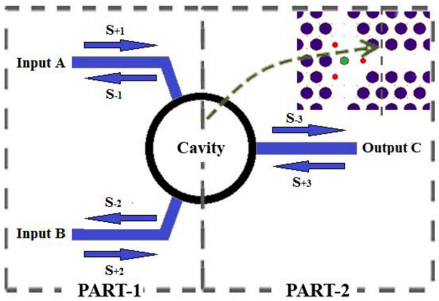

Fig. 3 *CMT-based abstract model of a Y-branch combiner*

power transfer from the input to the output ports need to be controlled. That is, the power of one input port should not be transferred to the output port when that at the other input port is unavailable. On the other hand, maximum power should be transferred to the output when powers at both the inputs are available. To achieve same, at first the cavity is conceptually segregated into two parts as shown in Fig. 3. Now, it can be stated as per the power transfer theory that the transfer of power from the part-1 to the part-2 can be maximised if the wave impedance of the output section of the part-1 matches that of the input section of the part-2. On contrary, the power transfer can be minimised by maximising the mismatch of the wave impedances of these parts. Therefore, these impedances have been calculated using the Bloch impedances as proposed as [21]

$$Z_B(z) = \frac{\int (E_y(x,z)/H_x(x,z))\mathrm{Re}P(x,z)\,\mathrm{d}x}{\int \mathrm{Re}P(x,z)dx} \quad (1)$$

where E, H and P are the electric field component, the magnetic field component and the Poynting vector, respectively. Thereafter, this Bloch impedance is averaged along the 'Z'-axis within the range of 2a length ending/starting at the boundary of the Part-1/Part-2 to calculate a real-valued wave impedance for the corresponding sections. That is

$$Z = (1/2a)\int Z_B(z)\,\mathrm{d}z \quad (2)$$

The equation calculates the input impedance of the Part-2, termed here as the channel impedance, as ~520 Ω. On the other hand, the Part-1 of the un-optimised cavity shows impedances close to that when either one or both of the inputs are excited with a continuous wave (CW) signal of wavelength 1550 nm representing the logic 'High'. This actually plays behind the ineffectiveness of the un-optimised cavity which leads to the availability of power when any/both of the inputs are exited. Now, in order to optimise the cavity for performing as an AND gate, a point defect is created by incorporating one circular silicon rod (termed as m1) in the junction of the channel waveguide. Moreover, including m1, other two rods adjacent to the cavity, i.e. m^2 and m^3, are considered in a single group, and their radius is considered as equal (r_m) and is set to 0.12a. Finally, the radius of the rod at the centre of the cavity, that is termed here as n, and that plays the most important role in performance control, is considered to be optimised for matching/mismatching the impedances of the two parts of the cavity while exiting only one/both of the inputs. Now, the radius 'r_n' of the rod 'n' is varied in the range 0.06a–0.31a, and the corresponding impedances are calculated using (2) for both the single- and double-port excitations. The same is shown in Fig. 4, which explores some interesting phenomena. The figure shows, through a black solid line, the real part of the impedance of output section of the Part-1, which is calculated with an excitation at only one of the input ports. So is referred here as 'impedance-with-single-excitation'. On the other hand, 'impedance-with-double-excitation' refers the same however when both the inputs are excited simultaneously. It can be seen from the figure that the impedance-with-single-excitation is significantly high and considerably different than the impedance-with-double-excitation. Actually, the

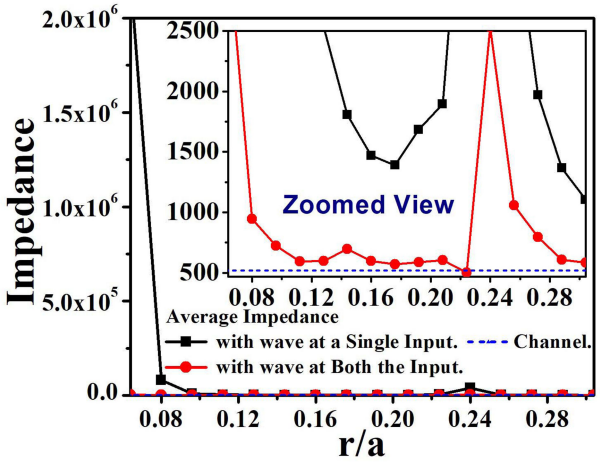

Fig. 4 *Wave impedance*

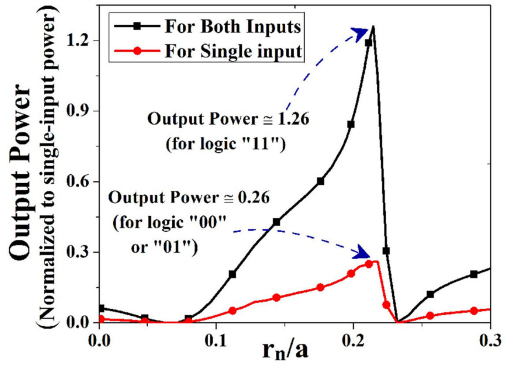

Fig. 5 *Output power curve for single and both inputs with respect to the various values of 'r_n'*

Table 1 Truth table and output power of AND gate

Input-A	Input-B	Output-C	Power level at the Output-C
0	0	0	0
0	1(P_{MAX})	0	0.26 P_{MAX}
1(P_{MAX})	0	0	0.26 P_{MAX}
1(P_{MAX})	1(P_{MAX})	1	1.26 P_{MAX}

impedance-with-double-excitation rapidly decreases from a high value and becomes closer to the channel impedance as r_n is increased beyond 0.08a. However, it again starts to increases drastically as r_n is taken larger than 0.22a. On contrary, the impedance-with-single-excitation in this range is much higher than the channel impedance and achieves minima in the range of r_n 0.16a–0.2a. Therefore, the cavity is expected to give the optimised performance when as r_n is close to 0.22a.

3 Performance analysis

Now, to verify the validity of the conceptual developments in the design phase/principle of the device, corresponding simulations are performed using a 2D finite-difference time-domain (FDTD) [22] method. The radius r_n is varied in the range 0–0.3a, and CW excitation(s) at the wavelength 1550 nm is (are) used in the input-port(s) to obtain the output power.

3.1 Power transfer

Interestingly, similar consequences, as described in the last section, are observed when the output powers are recorded for excitation in single and both the inputs. These observations are also shown in Fig. 5, which plots the output power (normalised to the maximum allowable power at a port) as a function of r_n (normalised to the lattice constant). It can be seen from Fig. 5 that the power at the

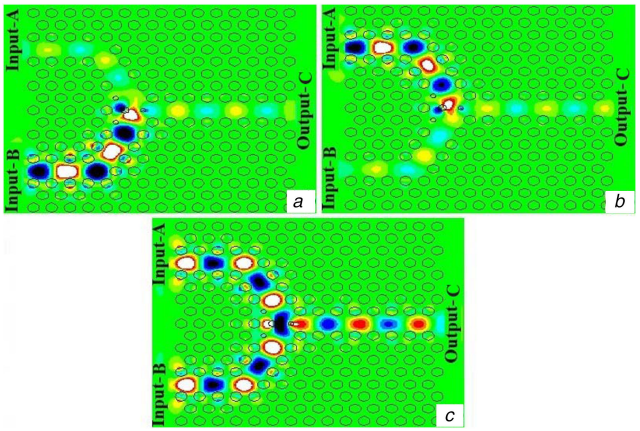

Fig. 6 *Electric field propagation in*
(a) TM mode in the input port-B depicting logic-01, ***(b)*** TM mode in the input port-A depicting logic-10, ***(c)*** TM mode in both the inputs depicting logic-11

output increases as the r_n increases in the range 0.075a–0.215a, when both the inputs are excited simultaneously, and the normalised-power eventually reaches to 1.26 at the end of this range. This is due to the fact that the impedance of part-1 is quite close to that of the part-2 (channel impedance) as has been observed in Fig. 4. Similarly, the steep rise in impedance of the part-1 above this range of r_n causes to reduce the output power. Moreover, the same range of r_n also sufficiently restricts the input power to reach the output port when only one of the inputs is exited. This is because of the sufficiently large difference between the channel impedance and the 'impedance-with-single-excitation' in this range. The normalised output power for this case becomes ≈0.26 at the r_n 0.215a.

3.2 Logic levels and propagation profile

Now, aided by the above phenomena, logic labels of the device are defined based on the optical power. The logic '1' is defined by the maximum allowed input power (P_{MAX}), which can be decided by the user. This flexibility is achieved as the operations of the device do not depend on any nonlinear medium. The P_{OH} and P_{OL} for the logic device [23] are intuitively considered as 0.6 P_{MAX} and 0.3 P_{MAX}, respectively. Propagation profiles for different kinds of inputs are simulated and presented in Fig. 6. Figs. 6a and b are, respectively, showing the propagation profile for the logics at the inputs A and B as '01' and '10'. It can be seen from these figures that the power at the output port is significantly less than that at the corresponding input. This output powers for these logic-inputs are 0.26 times of the input powers, as stated earlier, and can be considered as logic '0' as per our considerations. So are tabulated in the second and third row of Table 1, which presents the truth table of the device along with the corresponding power outputs. On the other hand, propagation profile for the logic input '11' is shown in Fig. 6c, which depicts a higher power output compared to an individual input (as stated earlier), and so is recorded in Table 1. The table also includes the entry for logic input '00'; however, the output power and logic in this case is obviously 0 as optical power has been applied to neither of the inputs.

3.3 Extinction ratio

ER is defined as the ratio of optical power at the output port when it is designated as the logic '1' to that when it is the logic '0' [24, 25]. Mathematically the ER can be represented as -

$$\mathrm{ER} = 10 \log_{10} \frac{P_1}{P_0} \tag{3}$$

where P_1 is the optical power at the output port for logic '1' and P_0 is the optical power at the output port for logic '0'. The ER is an important criterion as the bit error rate (BER) is inversely dependent and, simultaneously, the noise margin is directly

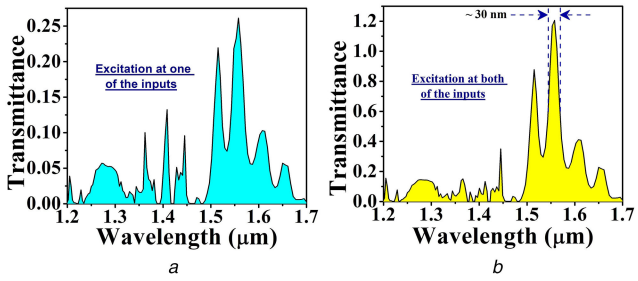

Fig. 7 *Transmittance characteristics at the output when the signal is applied to*
(a) a single input, ***(b)*** both the inputs

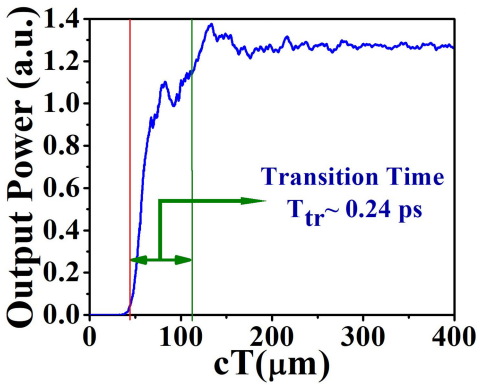

Fig. 8 *Time-evolving graph for the output power*

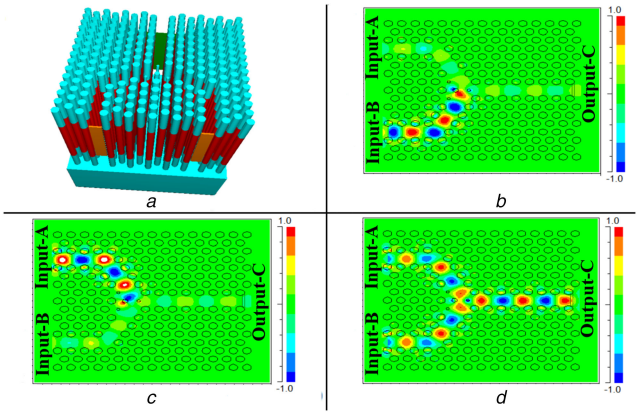

Fig. 9 *The 3D view of PhC-Slab and it's corresponding electric field profile at various input conditions*
(a) The 3D representation of AND gate, ***(b)*** Electric field profile at logic '01' inputs, ***(c)*** Electric field profile at logic '10' inputs, ***(d)*** Electric field profile at logic '11' inputs

dependent on it [24]. So it is calculated for the proposed device and is found as ≈ 6.9 dB at the targeted wavelength, i.e. 1550 nm, and for $r_n = 0.215a$.

3.4 Transmittance

Moreover, the TR of the device is also calculated for a range of wavelengths to evaluate its operational bandwidth. The TR at a particular wavelength is defined as the ratio of the power obtained at the output to the total power applied at the inputs, i.e.

$$\mathrm{TR} = \frac{P_{\mathrm{C}}}{(P_{\mathrm{A}} + P_{\mathrm{B}})} \tag{4}$$

Here, P_C is the power obtained at the output port C, and P_A and P_B are the input powers applied at input ports A and B, respectively.

Now, the TRs for two different types of logic combinations, i.e. '01' (or '10') and '11', are calculated for a long range of wavelengths, i.e. 1.2 to 1.7 μm, and are shown in Figs. 7*a* and *b*, respectively. The figure not only supports the previous observations for the 1550 nm wavelength but also shows that the logic definitions considered here remain validated for a 30 nm wide range of wavelengths around 1550 nm. This confirms an ≈ 4 THz the operational bandwidth of the device. Nevertheless, the constraints of the logic definitions can also be relaxed a little to enhance the bandwidth significantly.

3.5 Response time and data rate

Finally, the response time of the device, which is a determining factor for the propagation delay and data rate, has been calculated by time evolving curve of the output power. The calculation is performed by keeping all the other parameters such as normalised operating frequency (a/λ), r_m, and r_n constant to 0.46, 0.12a, and 0.21a, respectively. The calculation outcome has been shown in Fig. 8, which shows that the output power makes a transition from 1 to 90% of the maximum steady-state value (at that wavelength) in ≈0.24 ps (i.e. $\mathrm{cT_{tr}} \approx 115\,\mu$m, where '$c$' is speed of light in air and T_{tr} is the transition time). Now, considering this transition time is equal to the fall-time as well as rise-time, the proposed all-optical AND gate is expected to be operated at a bit rate >1 Tb/s ($1/4\mathrm{T_{tr}}$).

3.6 3D FDTD simulation on the final 2D-slab structure

In order to evaluate performance of the device in practical regime, the optimised model has been redesigned in a 2D-slab structure as shown in Fig. 9*a*. The structure is considered to be built on a silica slab, where silica rods are considered to be extended for 2 μm over the silica slab. The 5 μm long silicon rod structures are considered to be built above these silica rods, over which 2 μm long silica rods are again considered to be formed to maintain symmetry in the vertical direction of the structure. Rest of the design parameters are kept constant as previous. Now, this structure has been simulated using a 3D FDTD method under the excitation of input logic levels '01', '10' and '11'. The corresponding electric field distributions through the structure are shown in Figs. 9*a–d*, respectively. It is evident from these figures that the design and corresponding operations are persistent even in a finite 3D slab structure.

3.7 Comparative study with other optical AND gates

A comparative study on the performances of similar type of AND gates has been presented in Table 2. The following paragraph details the study as shown in the table. Andalib *et al.* [13] and Pashamehr *et al.* [15] have reported optical AND gates based on non-linear ring resonators. However, requirement of threshold input power, large footprint, low data-rate, and small output power at logic '1' make these devices less-attractive members within their family. Ring resonators and Y-shaped junctions have been used in [16, 26] to realise optical AND gates, in linear optical regime, having an ER of ≈6 dB. However, their footprint sizes are considerably large and the data-rates are moderate, which limit them to be chosen for a PIC application. Also, the self-collimation property of 2D PhC has been used in [27] to design an optical AND gate, but the ER and output power at logic '1' is comparatively small. On the other hand, Fasihi [17] has proposed an AND logic gate in a 2D square-lattice PhC using the properties of linear optics. Although the gate shows a good contrast ratio and its footprint is moderately small, the output power at logic '1' is substantially low. The work also sites applicability of cavity mode theory in its design but no explicit consideration of design methodology based on this theory has been mentioned. Similar strategies have been adopted by Rani *et al.* [18, 28]; however, they have considered a Y-shaped junction in different configurations of PhC to design their AND gate. Nevertheless, in contrast to the present work, none of the above reports adopts a specific methodology for designing/optimising their work. Thus, the application of impedance matching theory-based design and optimisation procedure has led us to achieve an AND gate that offers a high contrast ratio as 6.9 dB, a considerably high output

Table 2 Comparative study of different optical AND gates

Reference	Type of crystal[a]	Output power as logic-1[b]	Output power as logic-0[b]	Contrast ratio (dB)	Data rate, Tbps	Footprint size (μm^2)
[13]	RiA	0.656 I/P	0.13 I/P	6.93	0.12	253
[15]	RiA	—	—	—	—	396
[16]	RiA	—	—	6	0.208	572
[26]	RiA	1.0 I/P	0.25 I/P	6	0.83	863
[27]	RiA	0.75 I/P	0.25 I/P	4.9	—	100
[17]	RiA	0.5 I/P	0.125 I/P	6	—	296
[18]	HiS	1.58 I/P	0.395 I/P	6.02	0.83	—
[28]	HiS	1.63 I/P	0.414 I/P	5.95	3.33	64
this work	RiA	1.26 I/P	0.26 I/P	6.9	1	110

[a]RiA, rods in air; HiS, holes in slab.

[b]I/P is the maximum of the input powers.

power at logic '1', and a moderately high bit-rate in a considerably small footprint size.

4 Conclusion

A basic design of a PhC-based all-optical AND gate is proposed in this work. An impedance matching theory is devised and adopted to optimise the basic design of the AND gate. For the same, the design is divided into two parts, and impedances of both the parts are calculated. The radius of a rod in the Y-junction is varied and the corresponding variations in impedance are recorded for different types of input excitations (those represent different logic combinations). Finally, match/mismatch of impedances of the left section with that of the right one is enhanced at the desired/undesired logic combinations by optimising the radius. Thereafter different performance metrics such as power transfer, propagation profile, ER, TR and response time are evaluated for the optimised AND gate. Power transfer and TR of the device for different logic combinations ensure its logical operation as of the desired gate for a wideband (≈30 nm) of wavelengths. The high TR at the logic '1'output also confirms the repeatability of the device in a long chain of circuit. The high ER (≈6.9 dB) offered by the device makes it convenient for maintaining large noise margin and low BER. Also, the fast response time (≈0.25 ps) confirms the allowable bit rate in the range of 1 Tb/s.

Therefore, the proposed methodology successfully optimised a design of an all-optical AND gate for its better performance. The same is also expected to be useful for designing and optimising other kind of logic devices.

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