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Design and analysis of all-optical 1-to-2 line decoder based on linear photonic crystal

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Abstract: A new design of 1-to-2 line all-optical logic decoder has been proposed based on a two-dimensional photonic crystal (PhC) structure. The decoder operates based on the principle of optical interference within the PhC waveguides. An optical bias has been used to generate high-logic states at zero input conditions. Simulations explore a high contrast ratio, in the order of 11.3 dB, for both the output ports of the device. Response times have been calculated from the transient responses of the output ports, and are found as 0.65 and 0.77 ps for the ports 1 and 2, respectively. These results in a bit rate of ≃625 Gbps, considering the worst-case scenario. Phase sensitivity analysis has also been performed which shows that the device output is quite sensitive to the differences in phases of the bias and signals. However, a strategy has been proposed to make the same insensitive to the phase changes. Finally, the small footprint (in the order of 234 μm^2); standard operating wavelength; and silicon-based design of the decoder, along with its said merits, make the device highly potential for on-chip photonic-integrated-circuit applications.

1 Introduction

The last 50 years have seen exponential growth in the density of electronic transistors in integrated circuits. But now, this density of integration, as well as the speed of operation, of electronic transistors is rapidly driving to its saturation. Recently, photonics technology has been adopted by the technologists to drive out this saturation. In the recent past, photonics has contributed significantly in the applications of communication, biomedical, computer networking, aeronautics and so on. An all-optical photonic integrated circuit (PIC) [1] is one of the most potential technologies of the date and also believed to be inevitable in designing the components for future generation super computers [2]. Among the several design environments of all-optical PICs, the photonic crystal (PhC) [3–5] is one of the most prospective platforms as the light propagation in it is controlled by its unique phenomenon, i.e. photonic band gap. Since the last couple of decades, a number of researchers have developed several PhC based optical components, such as optical router [6], de-multiplexer [7, 8], decoder [9], polariser [10, 11], coupler [12, 13], logic gates [14–16], drop filter [17] and so on. Among these, the all-optical Boolean logic decoder is an important and challenging device. Some all-optical decoders have been reported in the recent literature based on a combination of non-linearity in PhC platform. For instance, Teimoori *et al.* [18] have demonstrated an optical decoder switch in the electro-optic domain. According to their report, the device can be operated at a maximum data rate of 10 Gbps along with a contrast ratio of 7.9 dB, which are not sufficient enough for future generation all-optical PICs. On the other hand, Serajmohammadi *et al.* [19] have reported a 1-to-2 line optical decoder switch based on photonic crystal ring resonator and non-linear Kerr effect, which requires high operating power for its operation. However, in spite of severing other approaches [9, 18–20] for designing all-optical decoders in the non-linear/electro-optic domain; they commonly incur several undesired requirement including high operating power; long interaction length; large non-linear coefficient of the matter and so on, which limit the integration density of PICs.

On the other hand, linear optical methodologies do not suffer from these disadvantages and are a promising approach to design highly integrable components for PICs. Linear optical phenomena, including multi-mode interference [21]; self-collimation [22]; light beam interference [23, 24] and so on, also offer several other advantages such as fast response time, high data rate, large operating bandwidth, high extinction ratio, low operating power and so on. Therefore, these motivations have driven the authors to design an all-optical 1:2 decoder in the linear optical regime, which is being reported in this paper.

The Boolean logic decoder is designed in a two-dimensional PhC structure, using the principle of optical interference. The finite difference time domain (FDTD) [25] method has been applied to simulate the characteristic of the device. The simulations explore that the device can operate at a high bit rate, which is over 600 Gbps. It also offers remarkable contrast ratios, over 11 dB, between the logic levels of its outputs. The other salient features of this design are its ultra-compact footprint, the absence of a requirement for threshold power, fast response time, operation at the ITU-standard optical wavelength, and simplicity of operation. Thus it is expected that the proposed decoder would prove itself as a suitable candidate for future photonic integrated circuits.

Remaining of the paper is organised as follows. Detail design of the decoder has been presented in the next section. The design has been analysed by considering the defect mode in the dispersion diagram of the PhC. The same section also incorporates FDTD simulations to analyse the operations of the device in different input conditions. In Section 3, the performances of the proposed structure have been evaluated by measuring several metrics, such as power variation; contrast ratio; response time and phase sensitivity. Finally, a conclusion of the paper has been drawn in the last section.

2 Device design and operating principle

The structure of the proposed all-optical decoder has been shown in Fig. 1. The structure is designed based on a two-dimensional photonic crystal platform, where dielectric silicon rods have been arranged in a triangular lattice. The background medium has been considered as air. The refractive index of the silicon rods and their radius are considered to be 3.42 and 0.32a, respectively, where 'a' (≡745 nm) is the lattice constant of the crystal. The structure of the decoder is designed in a small footprint of 234 μm^2 corresponding to a space of 25×20 number at silicon rods. The PhC structure (non-defect) has a band structure as in [26], abided by the same lattice spacing and radius of the rods, which shows a TM band gap

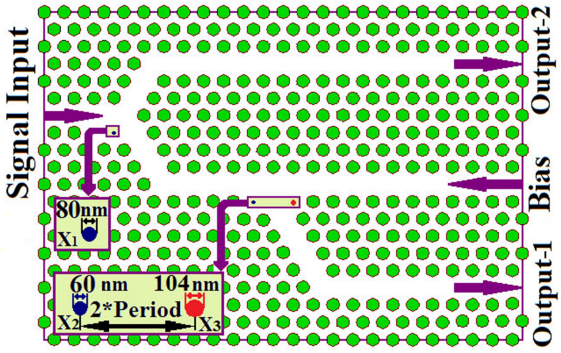


Fig. 1 *Schematic structure of 1*2 lines all-optical decoder*

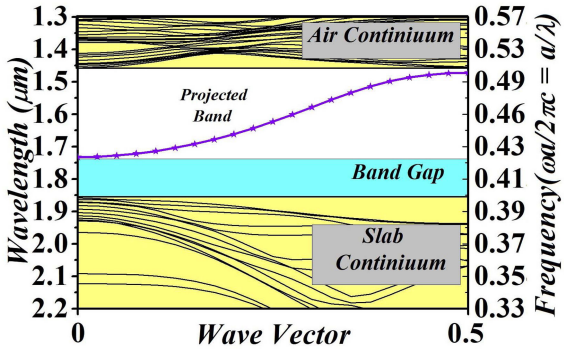
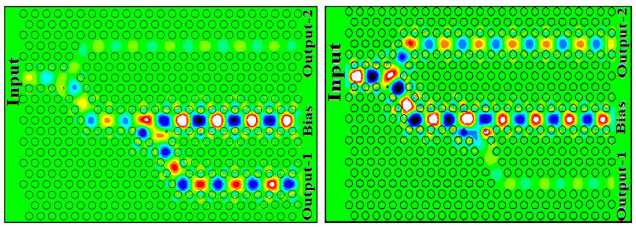


Fig. 2 *Dispersion diagram of photonic crystal W1 line defect waveguide at TM mode*



a *b*

Fig. 3 *Electric field propagation through the waveguides*
(a) TM signal is applied at the bias port only, ***(b)*** TM signals are applied at the bias port as well as the signal input port only

Table 1 Truth table and output power of 1*2 line decoder, when the bias-input is at logic '1'. All the inputs and outputs are calculated at a wavelength of 1550 nm

Signal input (1550 nm)	Output-1	Output-2	Power level at output-1[a]	Power level at output-2[a]
0	1	0	0.54Pi	0.04Pi
1	0	1	0.03Pi	0.55Pi

[a]Pi is the power at the signal-input port.

in the wavelength ranging from (a/0.52) to (a/0.41). However, a line defect waveguide in the Γ–M direction creates a propagating band within this band gap, and the band is recalculated and shown here in Fig. 2 for the convenience of the reader. The figure shows that the band allows propagation of wavelengths in the range of 1470–1720 nm, where the standard optical communication wavelength 1550 nm is expected to show maximum transmittance as it lies around the middle of the band.

Now, the device is designed considering one signal-input port, one bias-input port, and two output ports, as shown in Fig. 1. The bias input and the two output ports are designed on the opposite side of the input waveguide. The output-1 port is connected directly with the bias input port using a 120° bend waveguide with an intention that the majority of the power from the bias would leak/direct to this output. The junction of these ports forms a cavity like geometry, which is optimised to obtain the said objective. This optimisation is done by heuristically tuning the radius of the two rods, i.e. X_2 and X_3, at the corners of the junction, to 60 and 104 nm, respectively. Further, the bias waveguide meets to a 120° bend ahead of this junction. This bend forms one arm of the 'Y' junction, which is initiated from the signal-input port. The other arm of this 'Y' junction finally meets with the output-2 port. Moreover, the radius of one of the corner rods of this 'Y' junction is again optimised to 80 nm to direct the wave coming from the input port to the output-2 port whenever the bias input is available. Now, to ensure that the structure fulfils our objective, the FDTD method has been applied to obtain electric field distribution within the waveguide in different excitation conditions. As an initial condition, the bias input has been excited with a monochromatic continuous wave (CW) signal of wavelength 1550 nm and considered to be present throughout all different simulations.

After that, for the first case, the input port is chosen to be kept in a non-exciting condition that represents the logic state '0'. The corresponding electric field distribution is shown in Fig. 3*a*. It can be seen from the figure that most of the power from the bias input directs to the output-1 port. Although a small amount of the bias power also becomes available to the output-2 port, it is very less compared to the power available at the output-1. Time-averaged powers at the output-1 and output-2 ports are calculated and found, respectively, like 54 and 4% of the power available at the bias input. Therefore, it can be stated that the output-1 receives logic '1' and output-2 receives logic '0' in the case the input is excited with logic'0'.

Secondly, the signal-input port is excited by a monochromatic CW signal of wavelength 1550 nm with the same power and phase as of the bias-input, which is considered to be representing the logic'1'. The corresponding electric field propagation is shown in Fig. 3*b*, which shows that the majority of the power directs to the output-2 port, whereas the output-1 port receives a negligible power. This is because of the destructive interference at the junction of the bias-input and output-2 ports, which occurs when the input wave meets the bias wave at the opposite phase. Now, to verify the power delivery quantitatively, the time-averaged powers at both the ports are obtained and it is found that the output-2 receives a power about 55%, whereas the output-1 is delivered with a power of merely 3% of the input/bias power. This signifies that the output-1 receives the logic '0' state and output-2 has a logic '1' state whenever the input is excited with the logic '1' state. Hence, the total wave propagation characteristics can be summarised using the truth table (see Table 1) that establishes the operation of the device as a 1:2 line (logic) decoder.

Fabrication of the proposed structure may be made in the following way. A silica layer may be deposited on a silicon-on-insulator substrate using a plasma-enhanced chemical vapour deposition to create a vertical symmetry in the PhC slab. So may then be coated with a photoresist, followed by a patterning of the silicon rods by an e-beam lithography process. This should be followed by etching of photoresist, silica, and silicon in succession using a deep reactive ion etching (DRIE) procedure. A controlled DRIE may again be used to etch the silica bottom substrate to realise the final device structure.

3 Performance analysis

The performances of the decoder have been analysed through several metrics such as power variation; contrast ratio; response time and phase sensitivity, which are described in the following subsections.

3.1 Power variation

In this section, the dependency of output-powers for the variation in the powers at the signal-input has been calculated and is presented in Fig. 4. In these simulations, the power of the bias-input is kept as constant and that of the signal-input is varied from 0 to 1 in normalisation to the bias input. It can be seen from the figure that in the absence of the input signal power, the output port-1 and -2 receive, respectively, 54 and 4% of the bias-input power, which is in consistence to the previous discussion. Now, as

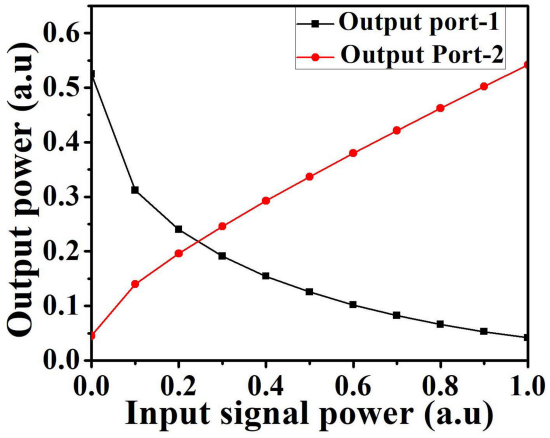


Fig. 4 *Output power versus signal-input power, while the bias-input is kept at logic '1'. The axes scales are normalised to the bias-input*

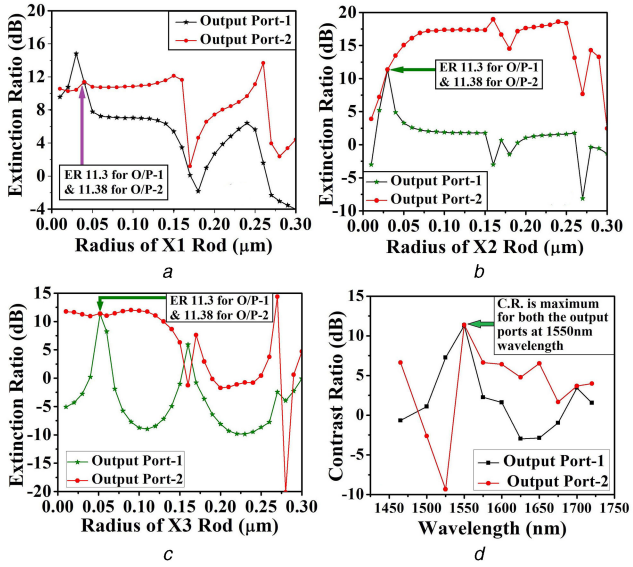


Fig. 5 *Contrast ratio of the output ports 1 and 2*
(a) By varying radius of the rod X_1, ***(b)*** By varying radius of the rod X_2, ***(c)*** By varying radius of the rod X_3, ***(d)*** By changing of wavelength

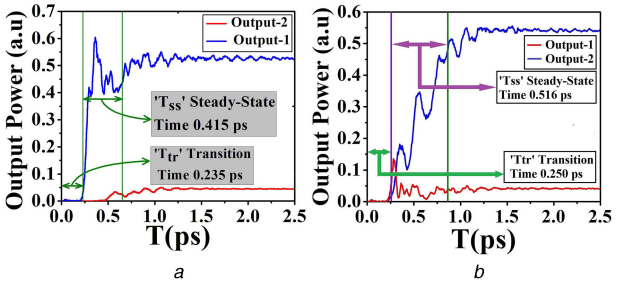


Fig. 6 *Time-evolving graph for the output power*
(a) When TM signal is applied at the signal input port, ***(b)*** When TM signal is not applied at the signal input port. The output-power scales are normalised to the bias-input

the power of the signal-input is increased, the destructive interference between the bias and the input signal is also increased at the junction of the bias and output-1 port. This, in turn, reduces the delivery of power to the output-1. However, a portion of the input power is transmitted to the output-2 unobstructed. Thus, power at the output-1 reduces and, at the same time, that at the output-2 increases with the increase in the input signal power. The same is reflected from the figure, which depicts that the output-1 and -2, in contrast to the previous case, receive ≃ 3% and 55% of the bias/input power while the input-signal is present in its full strength as of the bias.

Here, it is worth mentioning that the calculations presented here are based on the consideration that the device is a part of a larger PIC and the input/output power is launched/collected from the propagation plane of the device. Now, if the light is coupled from an optical fibre then the coupling efficiencies would influence the overall power transfer to the output ports. However, some parameters, including operational wavelength; phase sensitivity; or contrast ratio, would mostly be unaffected by this type of coupling and, thus, they can be considered as the intrinsic parameters of the device.

3.2 Contrast ratio

The contrast ratio is an important parameter for evaluating the performance of an output of a logic device/switch, as the noise margin is proportional to this parameter. Moreover, the bit error rate (BER) is inversely proportional to the contrast ratio of a device and, therefore, channel-performance is improved with a high contrast ratio [21]. The contrast ratio is defined as a ratio between the power at logic-1 to that at the logic-0. It is normally expressed as CR = 10Log $P1/P0$, where $P1$ and $P0$ indicate the signal power levels at the output port for logic-1 and logic-0, respectively.

Now, there are separate contrast ratios for two output ports as their configurations are different. Moreover, the contrast ratio for the individual ports is also dependent on the geometry of the three rods i.e. X_1, X_2, and X_3. Therefore, the contrast ratios of both the output ports have been calculated by varying the radius of these rods. However, during these calculations, the radius of each of these rods is varied while keeping that of the other rods as constant. Figs. 5*a–c* show the contrast ratios of the output ports with the variation of the radii of the rods X_1, X_2, and X_3, respectively. It can be seen from these figures that an optimum contrast ratios for the output port-1 and 2 are found as 11.3 and 11.4 dB, respectively, at a wavelength 1550 nm for the radius of X_1 as 40 nm, X_2 as 30 nm, and X_3 as 52 nm. This is the reason behind the choice of these typical values of radii in the design parameter.

Moreover, the contrast ratio is also a function of the wavelength due to the dispersion. Therefore, the same is calculated by varying the wavelength of the signal-input and bias-input ports simultaneously such that their wavelengths are always the same. The resultant contrast ratio for both the output ports is shown in Fig. 5*d*, which shows that the contrast ratio for both the ports becomes maximum for the wavelength 1550 nm.

3.3 Response time and data rate

Response time can be defined as the time required for the output to gain the 90% of its steady-state value from the initiation of the input that causes the change in the output. Here, the response times of the output ports have been calculated from their transient responses, in which the average optical powers at these ports are recoded with the evolving time. So are presented in Figs. 6*a* and *b*, respectively, for the output-1, in the absence of the input-signal, and output-2, in the presence of the input. Fig. 6*a* shows that, after initiation of the bias, the output-1 maintains approximately its previous value for around 0.23 ps (transition time) and takes a transition after that for ≃0.41 ps (steady-state time) to reach the 90% of its steady-state value, which is 54% of the bias power. Thus, altogether, the response time for the port is found as 0.65 ps. On the other hand, the output-2 takes a little longer time to arrive in its steady-state value, as can be seen from Fig. 6*b*. The figure depicts the transition, steady-state, and response time of the output-2 as 0.25, 0.52, and 0.77 ps, respectively. Thus, in the worst-case scenario, the maximum bit rate supported by the device can be estimated as 625 Gbps, considering that the fall-time is equal to the rise-time.

3.4 Phase sensitivity

The proposed decoder works based on the principle of constructive and destructive interferences and, hence, its outputs are greatly dependent on the phases of its input signals. Therefore, in this section, the dependency of output-powers for the difference in phases between the input signal and bias is studied. Some

simulations are performed considering logic '1'in both the inputs, however, the phase of the signal-input is gradually varied from 0° to 180° keeping the phase of the bias input constant at 0°. Average-powers at both the outputs are collected from these simulations and are plotted as normalisation to the input power in Fig. 7 with respect to the phase difference. It can be seen from the figure that the powers at the output-1 and -2 ports in zero phase difference are, respectively, ≃ 3 and ≃ 55% of the input power, and are consistent with the previous analyses. However, as the phase difference between the input and bias increases, the power at output 2 falls gradually and, at the same time, that at the output-1 port increases at a rapid rate. Finally, the output-1 starts to receive the logic level '1' while the phase difference of inputs becomes 180° and, thus the device loses its significance. The figure shows that the significance of operation of the proposed device can be sustained up to ≃ 20°

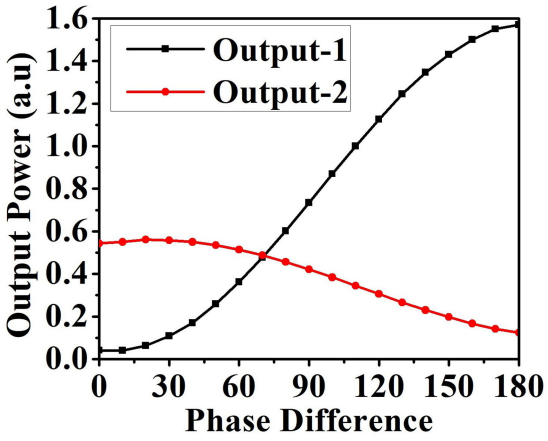


Fig. 7 *Output power of both the ports versus phase-difference of bias-input and signal-input while the bias-input is kept at logic '1'. The power-scale is normalised to the bias-input*

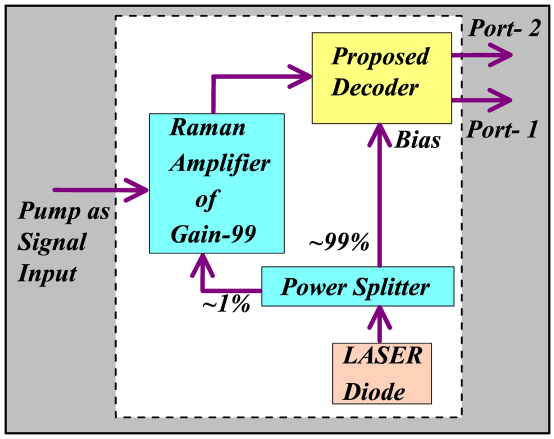


Fig. 8 *Schematic block diagram of the phase insensitive operation of the proposed decoder*

phase difference between the inputs. This depicts that the device is quite phased sensitive.

Nevertheless, additional arrangements can be adapted to make the decoder phase insensitive. The block diagram presented in Fig. 8 proposes one of such schemes. Here, a common source is considered to be taken for the bias and signal inputs. In ahead of this, a power splitter is used to tap a small portion (∼1%) of bias power for the signal input and the rest 99% of the power is directed to the bias port. Although the signal here would be in phase with the bias, its power would not be sufficient to create a significant destructive interference inside the proposed decoder; as can be inferred from Fig. 4. Hence, an integrable Raman amplifier [27] of gain 99 is used to amplify the input signal to its required strength for interference. Now, the pump of the amplifier can be considered as the new input signal. In the presence of this pump, the input of the proposed decoder receives a sufficient amount of signal-input power which would work as the logic '1' input. However, in the absence of the pump; the signal could not get amplified and provides power to the signal-input corresponding to the logic '0'. Further elaboration of this scheme is restricted here and may be discussed elsewhere in future.

3.5 Comparative study

The working principle of the decoder presented in work is based on linear optical operations, which, to the authors' best belief, is the first. Although there are several other decoders reported in the literature, most operates based on non-linear properties of optics. A comparative study among the all-optical logic decoders from differently reported literature has been presented in Table 2 based on their different performance and design matrices. The table shows that all the works except the one presented in this paper are implemented based on non-linear optical properties of materials. Hence, threshold optical powers are required for working of the decoders presented in those works, which is a strong bottleneck for their practical use. Moreover, it may also be observed from the table that the footprint-sizes of those decoders are comparatively larger than that of the decoder presented in this work. This increases the suitability of this decoder for its dense integration in PICs. In addition, contrast ratios of the ports of the decoder presented here are superior to the others enlisted in the table, which assist in reducing BER in a communication channel. Therefore, the comparison table concludes about the immense possibility of the decoder presented in this work towards achieving high data rate, low BER and high integration density, while its operation is not being constrained by a threshold optical power.

3.6 Extension strategy for higher order decoders

Fig. 9 describes the strategy of extending the proposed 1-to-2 decoder to a 2-to-4 decoder. As can be seen from the figure that, the design requires four all-optical AND gates (as proposed by the authors in [26]) and eight custom-designed power splitters for eight junction connections. However, the total design is quite complex and requires huge computational time for its simulation. Also, suitable power splitters for each junction are required to be

Table 2 Comparative study of different all-optical decoder switch

Ref.	Device design	Mode of operation	Contrast ratio, dB	Data rate, Tb/s	Threshold power kW/μm^2	Footprint size, μm^2
[9]	RiA[a]	non-linear	—	—	1	1906
[18]	SOA	non-linear	7.9 to 12	0.01	—	—
[19]	RiA[a]	non-linear	—	—	1.5	259
[28]	RiA[a]	non-linear	—	—	2	1746
[29]	RiA[a]	non-linear	—	0.2	—	1520
[30]	RiA[a]	non-linear	5.77	0.5	1	880
[31]	RiA[a]	non-linear	—	2	0.02	2352
[32]	RiA[a]	non-linear	6.8	0.16	0.13	1437
this work	RiA[a]	linear	11.3	0.625	—	234

[a]RiA: Rods in air PhC, '—' signifies non-availability of data.

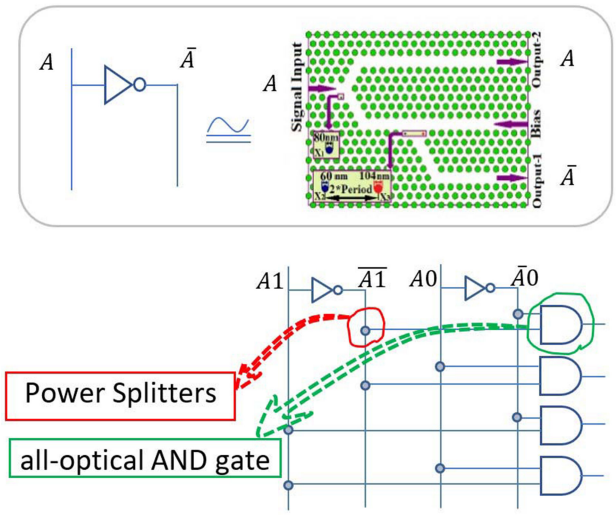


Fig. 9 *Schematic diagram of a 1-to-2 decoder to a 2-to-4 decoder*

designed for this implementation. Thus, the extension of this work towards implementation of 2-to-4 line or higher order decoder is beyond the scope of this work and would be discussed elsewhere in future work.

4 Conclusion

In this paper, a new design for a 1-to-2 line all-optical decoder has been proposed based on optical interference of light beams. The design uses a two-dimensional PhC structure where air-suspended dielectric rods are arranged in a triangular lattice. An additional optical-bias has been taken to provide a high-logic state in the absence of the input. Operation of the design as a Boolean logic decoder has been established through FDTD simulations. Different performance metrics, such as - power variation; contrast ratio; response time and phase sensitivity, have also been calculated to evaluate its compatibility for PICs. It has been seen that the device can perform better at an ITU standard wavelength, i.e. 1.55 µm. It also provides a fast response time of ≃0.77 ps, which leads to a data rate of ≃625 Gbps. Most importantly, the proposed device provides a high extinction ratio of ≃11.3 dB in a small footprint of 234 µm^2. Although, the design is phase sensitive, so can be mitigated by a combination of other optical components as discussed in the paper. Therefore, with these remarkable potentialities, the proposed decoder can efficiently be used to design future generation all-optical circuits in PICs.

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